CIPOS™ Tiny IM323

IM323-L6G/IM323-L6G2

Description

The CIPOS™ Tiny IM323 product group offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs. It is designed to control three phase AC motors and permanent magnet motors in variable speed drives for application like an air conditioning and refrigerator. The package concept is specially adapted to power application, which need good thermal conduction and electrical isolation, also EMI-save control and overload protection. The reverse conducting IGBTs are combined with an optimized SOI gate driver for excellent electrical performance.

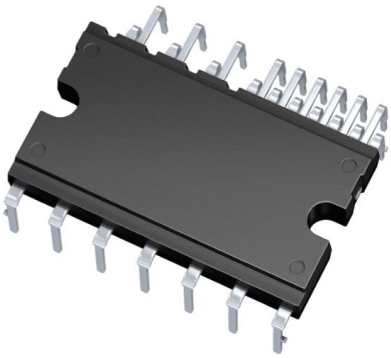
Features

Package

- Fully isolated Dual In-Line molded module
- Applied full-package
- Lead-free terminal plating; RoHS compliant

Inverter

- 600V Reverse conducting, RCD2 IGBT
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Allowable negative V_S potential up to -11V for signal transmission at V_{BS} = 15V
- Integrated bootstrap functionality
- Over current shutdown
- Built-in NTC thermistor for temperature monitoring
- Under-voltage lockout at all channels
- Low-side emitter pins accessible for phase current monitoring (open emitter)
- Sleep function
- Cross-conduction prevention
- All of 6 switches turn off during protection



Potential applications

Air conditioning and Home appliances

Industrial drives

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Table 1 Product information

Base part number	Package type	Standard pack		Remark
		Form	MOQ	
IM323-L6G	DIP 33x19	15 pcs / Tube	240 pcs	
IM323-L6G2	DIP 33x19	15 pcs / Tube	240 pcs	Short lead

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1 Internal electrical schematic

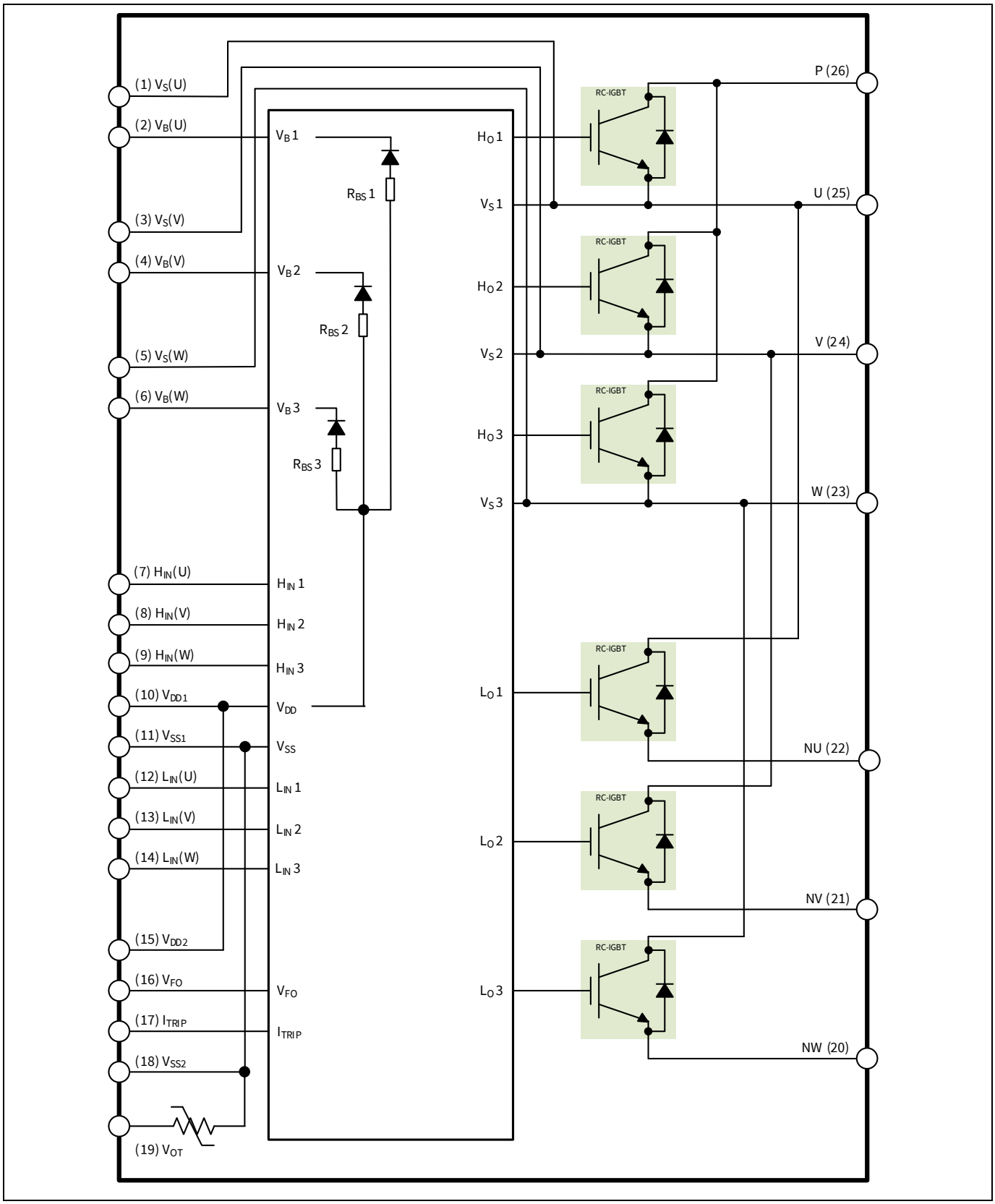


Figure 1 Internal electrical schematic

2 Pin description

2.1 Pin assignment

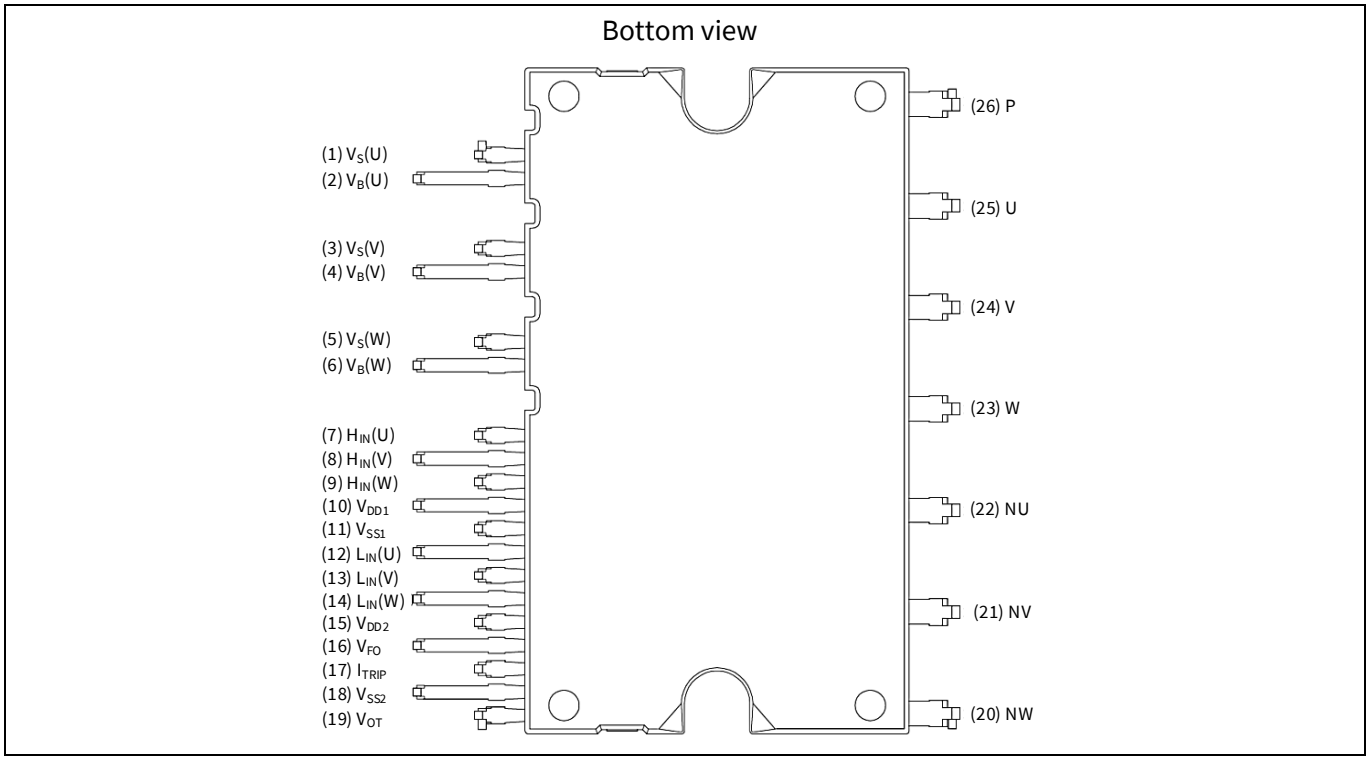


Figure 2 Pin configuration

Table 2 Pin assignment

Pin number	Pin name	Pin description
1	V_S(U)	U-phase high-side floating IC supply offset voltage
2	V_B(U)	U-phase high-side floating IC supply voltage
3	V_S(V)	V-phase high-side floating IC supply offset voltage
4	V_B(V)	V-phase high-side floating IC supply voltage
5	V_S(W)	W-phase high-side floating IC supply offset voltage
6	V_B(W)	W-phase high-side floating IC supply voltage
7	H_{IN}(U)	U-phase high-side gate driver input
8	H_{IN}(V)	V-phase high-side gate driver input
9	H_{IN}(W)	W-phase high-side gate driver input
10	V_{DD1}	Low-side control supply
11	V_{SS1}	Low-side control negative supply
12	L_{IN}(U)	U-phase low-side gate driver input
13	L_{IN}(V)	V-phase low-side gate driver input
14	L_{IN}(W)	W-phase low-side gate driver input
15	V_{DD2}	Low-side control supply
16	V_{FO}	Fault-output
17	I_{TRIP}	Over-current shutdown input

Pin description

Pin number	Pin name	Pin description
18	V_{SS2}	Low-side control negative supply
19	V_{OT}	Temperature output
20	NW	W-phase low-side emitter
21	NV	V-phase low-side emitter
22	NU	U-phase low-side emitter
23	W	Motor W-phase output
24	V	Motor V-phase output
25	U	Motor U-phase output
26	P	Positive bus input voltage

2.2 Pin description

H_{IN} (U, V, W) and L_{IN} (U, V, W) (High-side pins, Pin 7 – 9 and Low-side pins, Pin 12 - 14)

These pins are positive logic and they are responsible for the control of the integrated IGBTs. The schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Pull-down resistor of about 5 kΩ is internally provided to pre-bias inputs during supply start-up. Input schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time $t_{FIL,IN}$ The filter acts according to Figure 4. It is not recommended for proper work to provide input pulse-width lower than 1 µs.

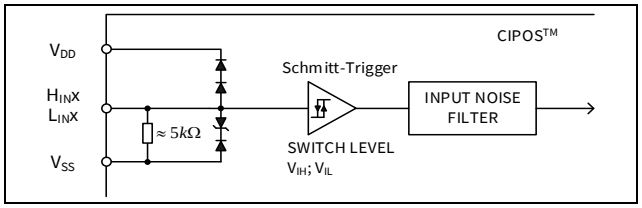


Figure 3 Input pin structure

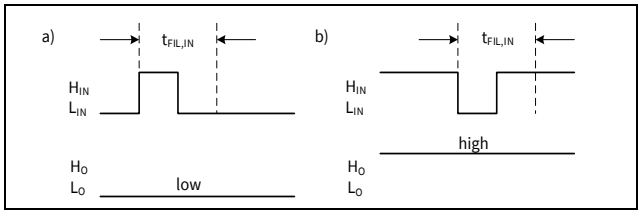


Figure 4 Input filter timing diagram

The integrated gate driver provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e. H_O1 and L_O1, H_O2 and L_O2, H_O3 and L_O3). When two inputs of a same leg are activated, only former activated one is activated so that the leg is kept steadily in a safe state.

A minimum deadtime insertion of typically 360 ns is also provided by driver IC, in order to reduce cross-conduction of the external power switches.

V_{FO} (Fault-output, Pin 16)

The V_{FO} pin indicates a module failure in case of under-voltage at pin V_{DD} or in case of triggered over-current detection at I_{TRIP}. An external pull-up resistor is required.

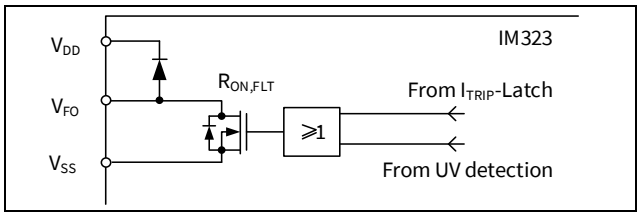


Figure 5 Internal circuit at pin V_{FO}

The sleep function is activated after each trigger of I_{TRIP} or under-voltage lockout. A new edge input signals is mandatory to activate gate drives after fault-clear time as shown in Figure 10.

I_{TRIP} (Over-current detection function, Pin 17)

The IM323 product group provides an over-current detection function by connecting the I_{TRIP} input with the IGBT current feedback. The I_{TRIP} comparator

threshold (typ. = 0.525 V) is referenced to V_{SS}. An input noise filter (t_{ITRIP} = typ. 530 ns) prevents the driver to detect false over-current events.
Over-current detection generates a shutdown of outputs of the gate driver. Fast track shutdown function allows low-side outputs to be turned off faster than high-side outputs about 200 ns. The fault-clear time is set to minimum 100 µs.

V_{DDX}, V_{SSX} (Control supply and reference, Pin 10(15) and reference, Pin 11(18))

V_{DD} is the control supply and it provides power both to input logic and to output power stage. Input logic is referenced to V_{SS} ground.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of V_{DDUV+} = 12.4 V is present.

The IC shuts down all the gate drivers power outputs, when the V_{DD} supply voltage is below V_{DDUV-} = 11.5 V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

V_B (U, V, W) and V_S (U, V, W) (High-side supplies, Pin 1 - 6)

V_B to V_S is the high-side supply voltage. The high-side circuit can float with respect to V_{SS} following the external high-side power device emitter voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The under-voltage detection operates with a rising supply threshold of typical V_{BSUV+} = 11.5 V and a falling threshold of V_{BSUV-} = 10.7 V.

V_S (U, V, W) provide a high robustness against negative voltage in respect of V_{SS} of -50 V transiently. This ensures very stable designs even under rough conditions.

NW, NV, NU (Low-side emitter, Pin 20 - 22)

The low-side emitters are available for current measurements of each phase leg. It is recommended to keep the connection to pin VSS as short as possible in order to avoid unnecessary inductive voltage drops.

W, V, U (High-side emitter and low-side collector, Pin 23 - 25)

These pins are connected to motor U, V, W input pins.

P (Positive bus input voltage, Pin 26)

The high-side IGBTs are connected to the bus voltage. It is noted that the bus voltage does not exceed 450 V.

3 Absolute maximum ratings

(V_{DD} = 15V and T_J = 25°C, if not stated otherwise)

3.1 Module section

Description	Symbol	Condition	Value	Unit
Storage temperature range	T_{STG}		-40 ~ 125	°C
Operating case temperature	T_C	Refer to Figure 7	-40 ~ 125	°C
Operating junction temperature	T_J		-40 ~ 150	°C
Maximum junction temperature[1]	$T_{J, switch, max}$		175	°C
Isolation voltage	V_{ISO}	1 min, RMS, f = 60 Hz	2000	V

3.2 Inverter section

Description	Symbol	Condition	Value	Unit
Maximum blocking voltage	V_{CES}	I_C = 250 µA	600	V
DC link supply voltage of P - N	V_{PN}	Applied between P - N	450	V
DC link supply voltage (surge) of P - N	$V_{PN(Surge)}$	Applied between P - N	500	V
Collector current[2]	I_C	T_C = 25°C, T_J < 150°C	±15	A
Maximum peak collector current	I_{CP}	T_C = 25°C, T_J < 150°C, less than 1 ms	±30	A
Power dissipation per IGBT	P_{tot}		27	W
Short circuit withstand time	t_{SC}	V_{DD} = 15 V, V_{DC} ≤ 400 V, T_J ≤ 150°C	3	µs

3.3 Control section

Description	Symbol	Condition	Value	Unit
High-side offset voltage	V_S		600	V
Repetitive peak reverse voltage of bootstrap diode	V_{RRM}		600	V
Module control supply voltage	V_{DD}	Applied between V_{DD} - V_{SS}	-1 ~ 20	V
High-side floating supply voltage (V_B reference to V_S)	V_{BS}	Applied between V_B - V_S	-1 ~ 20	V
Input voltage (L_{IN}, H_{IN}, I_{TRIP})	V_{IN}		-1 ~ V_{DD} + 0.3	V
Fault-output voltage	V_{FO}		-1 ~ V_{DD} + 0.3	V

[1]The maximum junction temperature rating of built in power chips is 175℃ under condition: max. 10 sec, every 10 min, max. 1 hrs cumulative over lifetime.
[2]Limited by junction temperature.

4 Thermal characteristics

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Single IGBT thermal resistance, junction-case	R_{thJC}	Low-side U-phase (See Figure 7 for T_C measurement point)	-	-	4.7	K/W
Single diode thermal resistance, junction-case	$R_{thJC, D}$		-	-	7.4	K/W

5 Recommended operation conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified.

Description	Symbol	Value			Unit
		Min.	Typ.	Max.	
DC link supply voltage of P - N	V_{PN}	0	300	450	V
Low-side supply voltage	V_{DD}	13	15	17.5	V
High-side floating supply voltage (V_B vs. V_S)	V_{BS}	13		17.5	V
Logic input voltages L_{IN}, H_{IN}, I_{TRIP}	V_{IN} V_{ITRIP}	0	-	5	V
Inverter PWM carrier frequency	f_{PWM}	-	-	20	kHz
External dead time between H_{IN} & L_{IN}	DT	1	-	-	µs
Voltage between V_{SS} - N (including surge)	V_{COMP}	-5	-	5	V
Minimum input pulse width	$PW_{IN(ON)}$, $PW_{IN(OFF)}$	0.7	-	-	µs
Control supply variation	ΔV_{BS} ΔV_{DD}	-1 -1	- -	1 1	V/µs

6 Static parameters

(V_{DD} = 15 V and T_J = 25°C, if not stated otherwise)

6.1 Inverter section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Collector-emitter saturation voltage	$V_{CE(Sat)}$	I_C = 12 A, T_J = 25°C I_C = 12 A, T_J = 150°C	- -	2.00 2.35	2.40 -	V
Collector-emitter leakage current	I_{CES}	V_{CE} = 600 V	-	-	1	mA
Diode forward voltage	V_F	I_C = 12 A, T_J = 25°C I_C = 12 A, T_J = 150°C	- -	1.95 2.00	2.30 -	V

6.2 Control section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Logic "1" input voltage (L_{IN}, H_{IN})	V_{IH}		1.7	2.0	2.3	V
Logic "0" input voltage (L_{IN}, H_{IN})	V_{IL}		0.7	0.9	1.1	V
I_{TRIP} positive going threshold	$V_{IT,TH+}$		475	525	570	mV
I_{TRIP} input hysteresis	$V_{IT,HYS}$		45	70	-	mV
V_{DD} and V_{BS} supply under-voltage positive going threshold	V_{DDUV+}		11.5	12.4	13.1	V
	V_{BSUV+}		10.6	11.5	12.2	
V_{DD} and V_{BS} supply under-voltage negative going threshold	V_{DDUV-}		10.6	11.5	12.3	V
	V_{BSUV-}		9.7	10.7	11.7	
V_{DD} and V_{BS} supply under-voltage lockout hysteresis	V_{DDUVH}, V_{BSUVH}		0.5	0.9	-	V
Quiescent V_{BSx} supply current (V_{BSx} only)	I_{QBS}	V_{HIN} = 0 V	-	-	300	µA
Quiescent V_{DD} supply current (V_{DD} only)	I_{QDD}	V_{LIN} = 0 V, V_{HINX} = 5 V	-	-	1.1	mA
Input bias current for L_{IN}, H_{IN}	I_{IN+}	V_{IN} = 5 V	-	1.1	1.7	mA
Input bias current for I_{TRIP}	I_{ITRIP+}	V_{ITRIP} = 5 V	-	68	185	µA
Input bias current for V_{FO}	I_{FO}	V_{FO} = 5 V, V_{ITRIP} = 0 V	-	60	-	µA
V_{FO} output voltage	V_{FO}	I_{FO} = 10 mA, V_{ITRIP} = 1 V	-	0.35	-	V
Bootstrap diode forward voltage	$V_{F,BSD}$	I_F = 0.3 mA	-	1.0	-	V
Bootstrap diode resistance	R_{BSD}	Between V_F = 4 V and V_F = 5 V	-	37	-	Ω

7 Dynamic parameters

(V_{DD} = 15V and T_J = 25°C, if not stated otherwise)

7.1 Inverter section

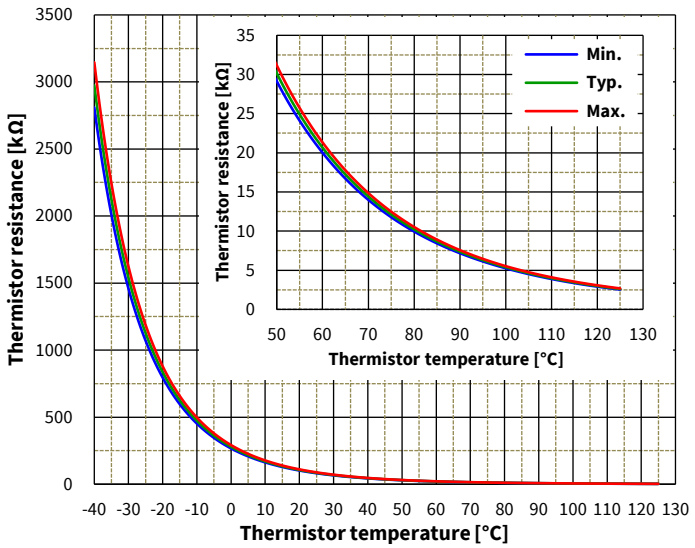
Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Turn-on propagation delay time	t_{on}	$V_{LIN, HIN}$ = 5 V, I_C = 15 A, V_{DC} = 300 V	-	720	-	ns
Turn-on rise time	t_r		-	40	-	ns
Turn-on switching time	$t_{c(on)}$		-	130	-	ns
Reverse recovery time	t_{rr}		-	135	-	ns
Turn-off propagation delay time	t_{off}	$V_{LIN, HIN}$ = 5 V, I_C = 15 A, V_{DC} = 300 V	-	805	-	ns
Turn-off fall time	t_f		-	25	-	ns
Turn-off switching time	$t_{c(off)}$		-	60	-	ns
Short circuit propagation delay time	t_{SCP}	From $V_{IT, TH+}$ to 10% I_{SC}	-	1250	-	ns
IGBT turn-on energy (includes reverse recovery of diode)	E_{on}	V_{DC} = 300 V, I_C = 15 A T_J = 25°C 150°C	- -	365 515	- -	µJ
IGBT turn-off energy	E_{off}	V_{DC} = 300 V, I_C = 15 A T_J = 25°C 150°C	- -	170 230	- -	µJ
Diode recovery energy	E_{rec}	V_{DC} = 300 V, I_C = 15 A T_J = 25°C 150°C	- -	60 120	- -	µJ

7.2 Control section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input filter time I_{TRIP}	t_{ITRIP}	V_{ITRIP} = 1 V	-	530	-	ns
Input filter time at L_{IN}, H_{IN} for turn on and off	$t_{FIL, IN}$	$V_{LIN, HIN}$ = 0 V or 5 V	-	290	-	ns
Fault clear time after I_{TRIP}-fault	$t_{FLT, CLR}$	V_{ITRIP} = 1 V, $V_{pull-up}$ = 5 V (R = 1 MΩ, C = 2 nF)	100	280	-	µs
I_{TRIP} to fault propagation delay	t_{FLT}	$V_{LIN, HIN}$ = 0 or 5 V, V_{ITRIP} = 1 V	-	680	1000	ns
Internal deadtime	DT_{IC}	V_{IN} = 0 or V_{IN} = 5 V	-	360	-	ns
Matching propagation delay time (On & Off) all channels	M_T	External dead time > 500 ns	-	20	-	ns

8 Thermistor characteristics

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Resistance	R_{NTC}	T_{NTC} = 25°C	-	85	-	kΩ
B-constant of NTC (Negative Temperature Coefficient) thermistor	B (25/100)		-	4092	-	K



Temp. [°C]	$R_{Min.}$ [kΩ]	$R_{Typ.}$ [kΩ]	$R_{Max.}$ [kΩ]
50	29.151	30.157	31.178
60	20.018	20.669	21.329
70	13.994	14.424	14.858
80	9.946	10.234	10.523
90	7.177	7.373	7.569
100	5.253	5.388	5.523
110	3.884	3.99	4.096
120	2.908	2.991	3.075
125	2.527	2.601	2.676

Figure 6 Thermistor resistance – temperature curve and table

(For more information, please refer to application note 'AN2021-04 CIPOS™ Tiny IM323 application note'.)

9 Mechanical characteristics and ratings

Description	Condition		Value			Unit
			Min.	Typ.	Max.	
Mounting torque	M3 screw and washer		0.59	0.69	0.78	N·m
Terminal strength pull	Control terminal: Load 5 N Power terminal: Load 10 N	JEITA-ED-4701	10	-	-	s
Terminal strength bending	Control terminal: Load 2.5 N Power terminal: Load 5 N 90degree bend	JEITA-ED-4701	2	-	-	times
Backside curvature	Refer to Figure 8		0	-	110	µm
Weight			-	5.6	-	g

10 Qualification information

UL certification	File number: E314539	
Moisture sensitivity level	-	
RoHS compliant	Yes (Lead-free terminal plating)	
ESD (Electrostatic Discharge)	HBM (Human body model)	2000 V
	CDM (Charged device model)	500 V

11 Diagrams and tables

11.1 T_C measurement point

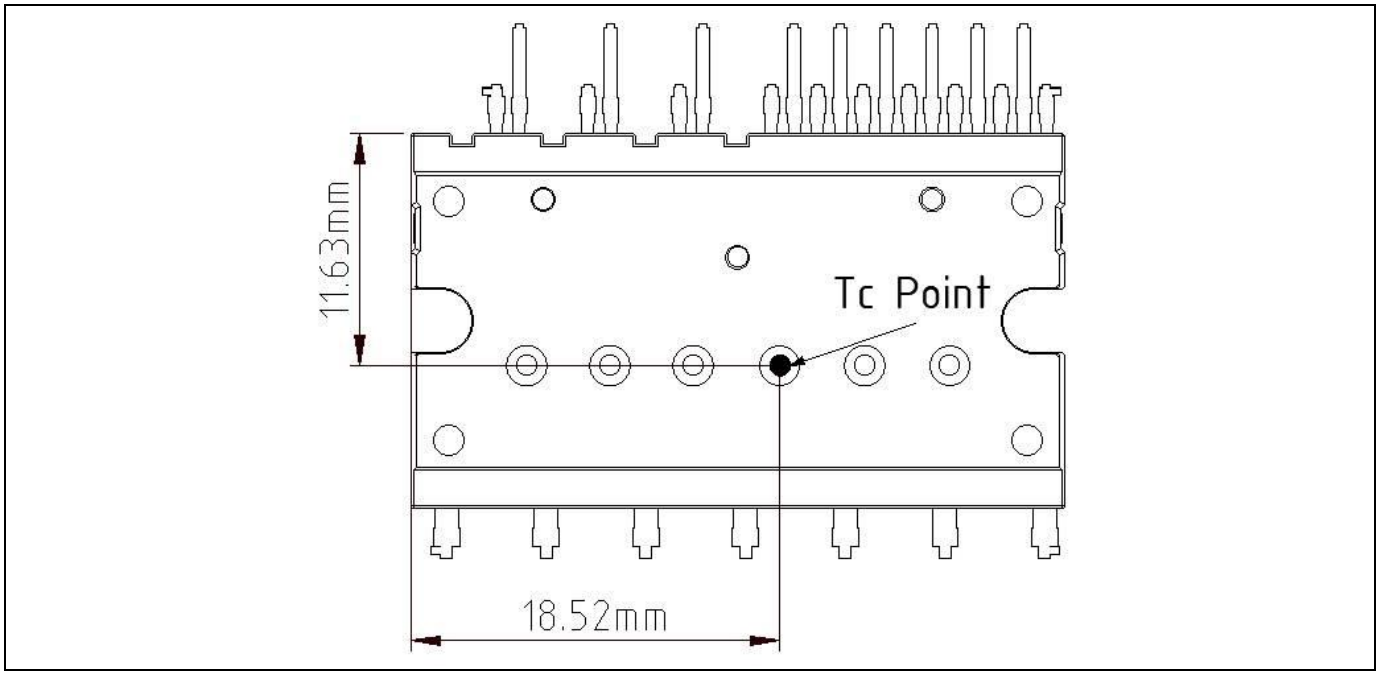


Figure 7 T_C measurement point[1]

11.2 Backside curvature measurement point

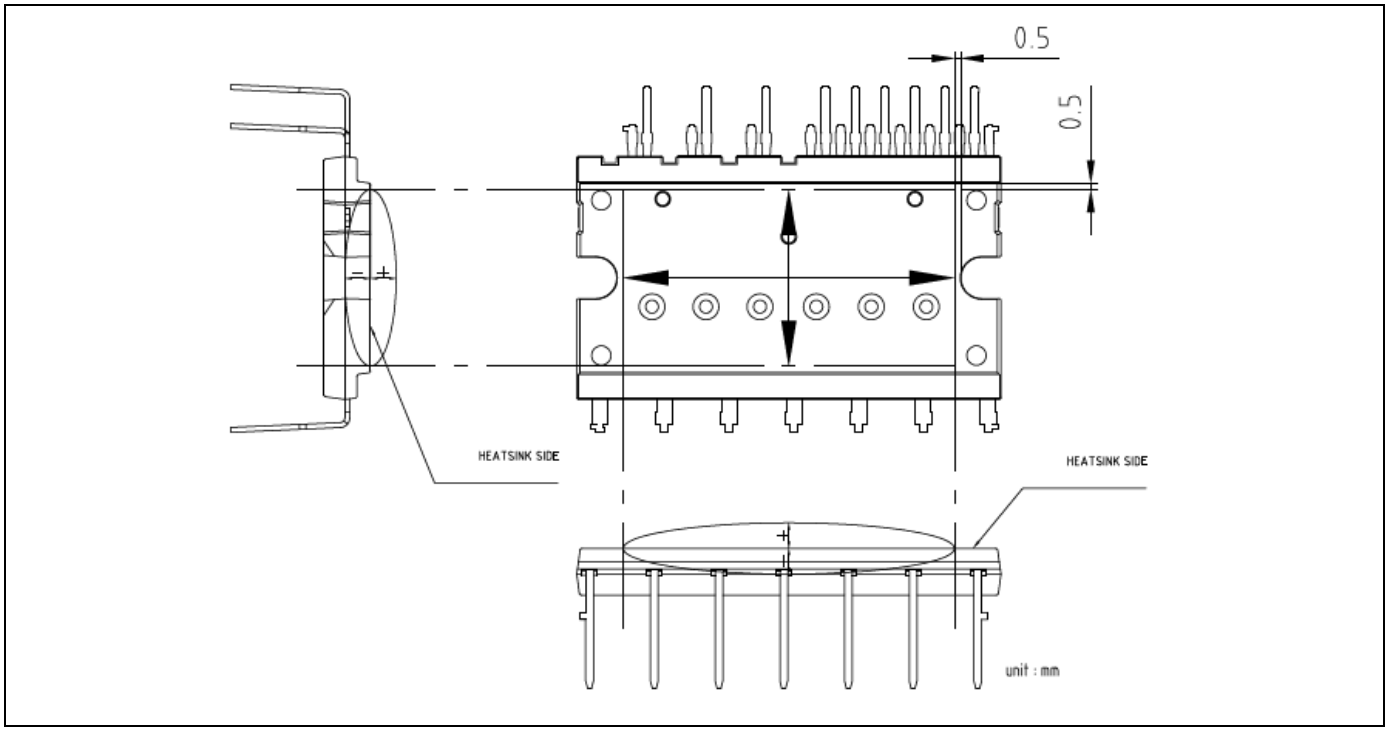


Figure 8 Backside curvature measurement position

[1]Any measurement except for the specified point in Figure 7 is not relevant for the temperature verification and brings wrong or different information.

11.3 Switching time definition

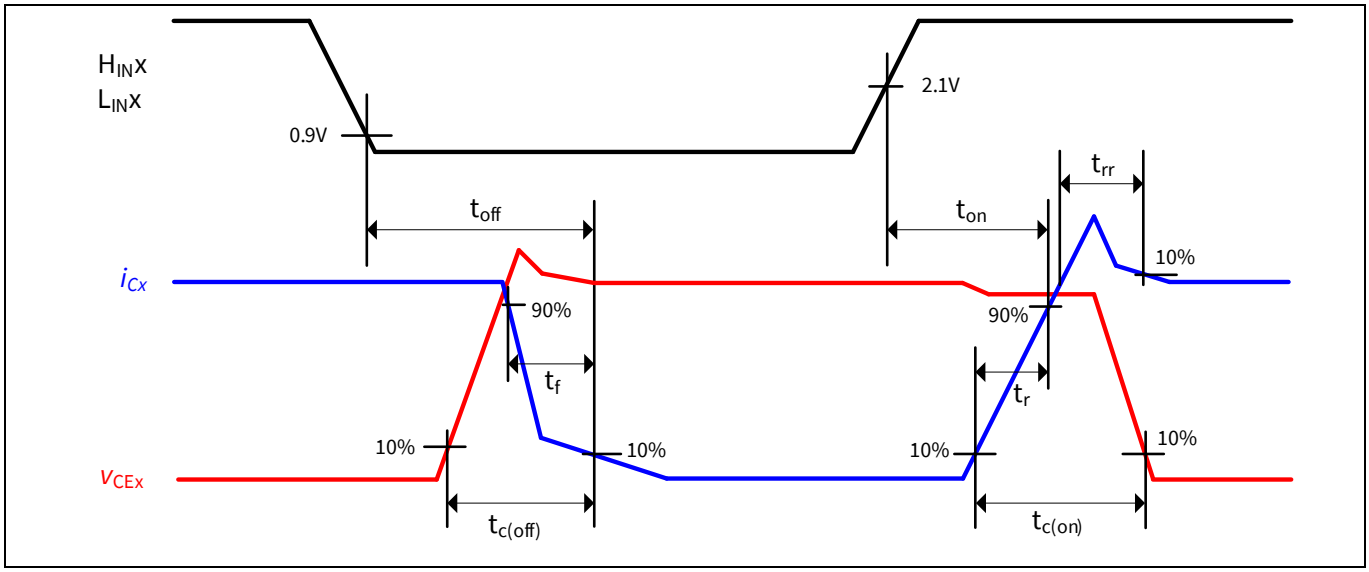


Figure 9 Switching times definition

11.4 Sleep function timing diagram

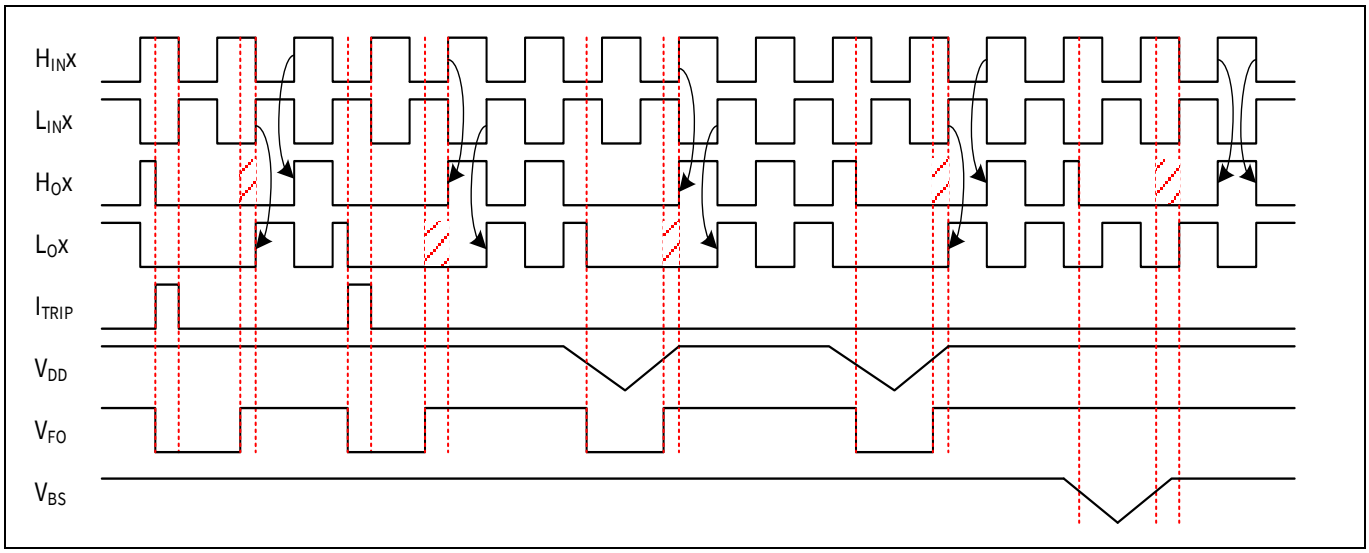


Figure 10 Sleep function timing diagram

12 Application guide

12.1 Typical application schematic

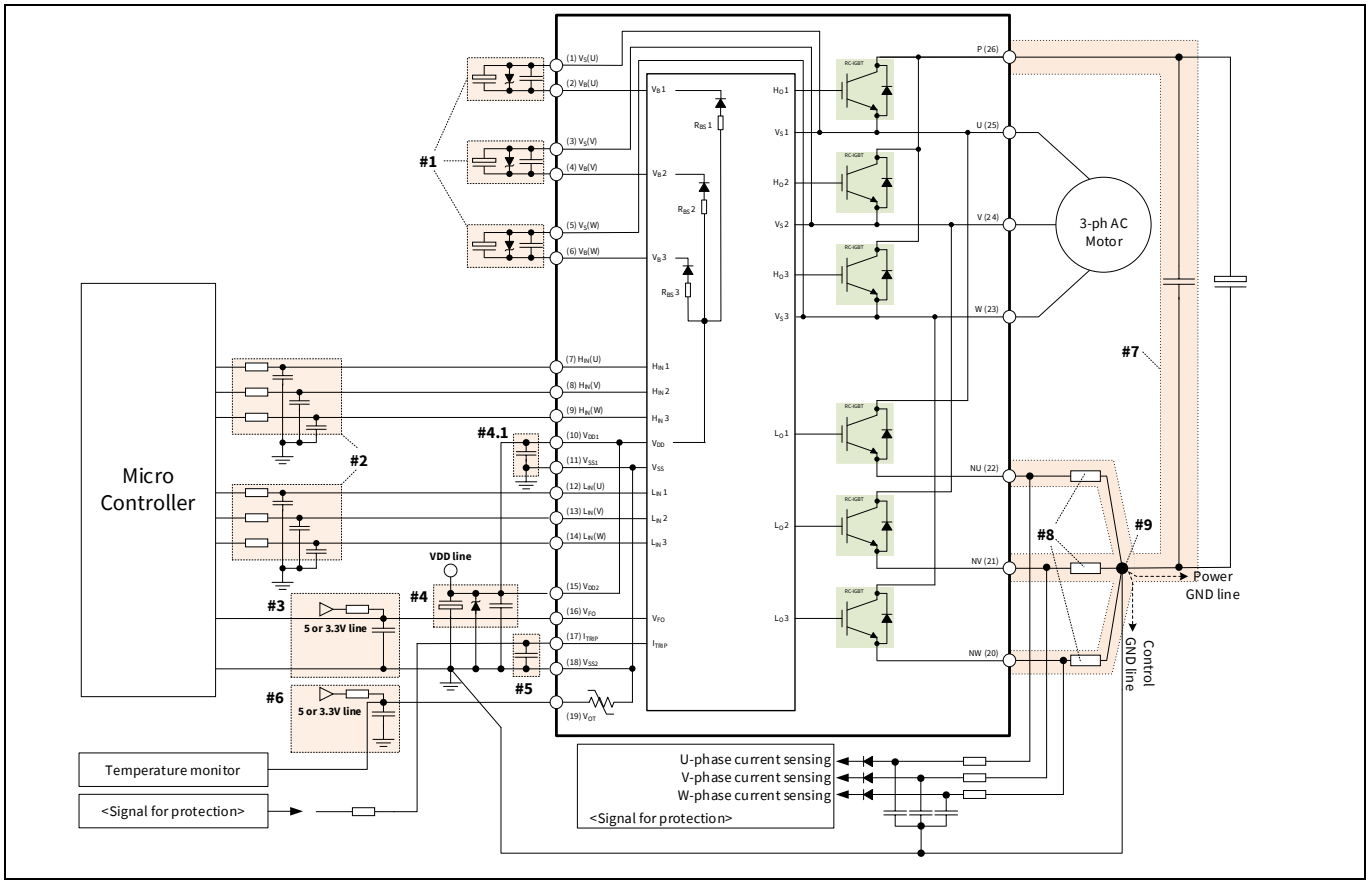


Figure 11 Typical application circuit

1. V_B-V_S circuit
   - Capacitor and Zener diode for high-side floating supply voltage should be placed as close to V_B and V_S pins as possible.
2. Input circuit
   - To reduce input signal noise by high speed switching, the R_{IN} and C_{IN} filter circuit should be mounted. (100 Ω, 1 nF)
   - C_{IN} should be placed as close to V_{SS} pin as possible.
3. V_{FO} circuit
   - V_{FO} pin is open drain configuration. This terminal should be pulled up to the bias voltage of the 5 V/3.3 V through a proper resistor.
   - It is recommended that RC filter is placed close to the controller.
4. V_{DD}-V_{SS} circuit
   - Capacitor and Zener diode for control supply voltage should be placed as close to V_{DD2} and V_{SS2} pins as possible.
5. I_{TRIP} circuit
   - To prevent protection function errors, C_{ITRIP} should be placed as close to I_{TRIP} and V_{SS2} pins as possible.
6. V_{OT} circuit
   Capacitor should be placed as close to V_{OT} and V_{SS} pins as possible due to V_{OT} voltage is analog voltage.
7. Snubber capacitor
   - The wiring between IPM and snubber capacitor including shunt resistor should be as short as possible.
8. Shunt resistor
   - The shunt resistor of SMD type should be used for reducing its stray inductance.
9. Ground pattern
   - Ground pattern should be separated at only one point of shunt resistor as short as possible.

13 Package outline

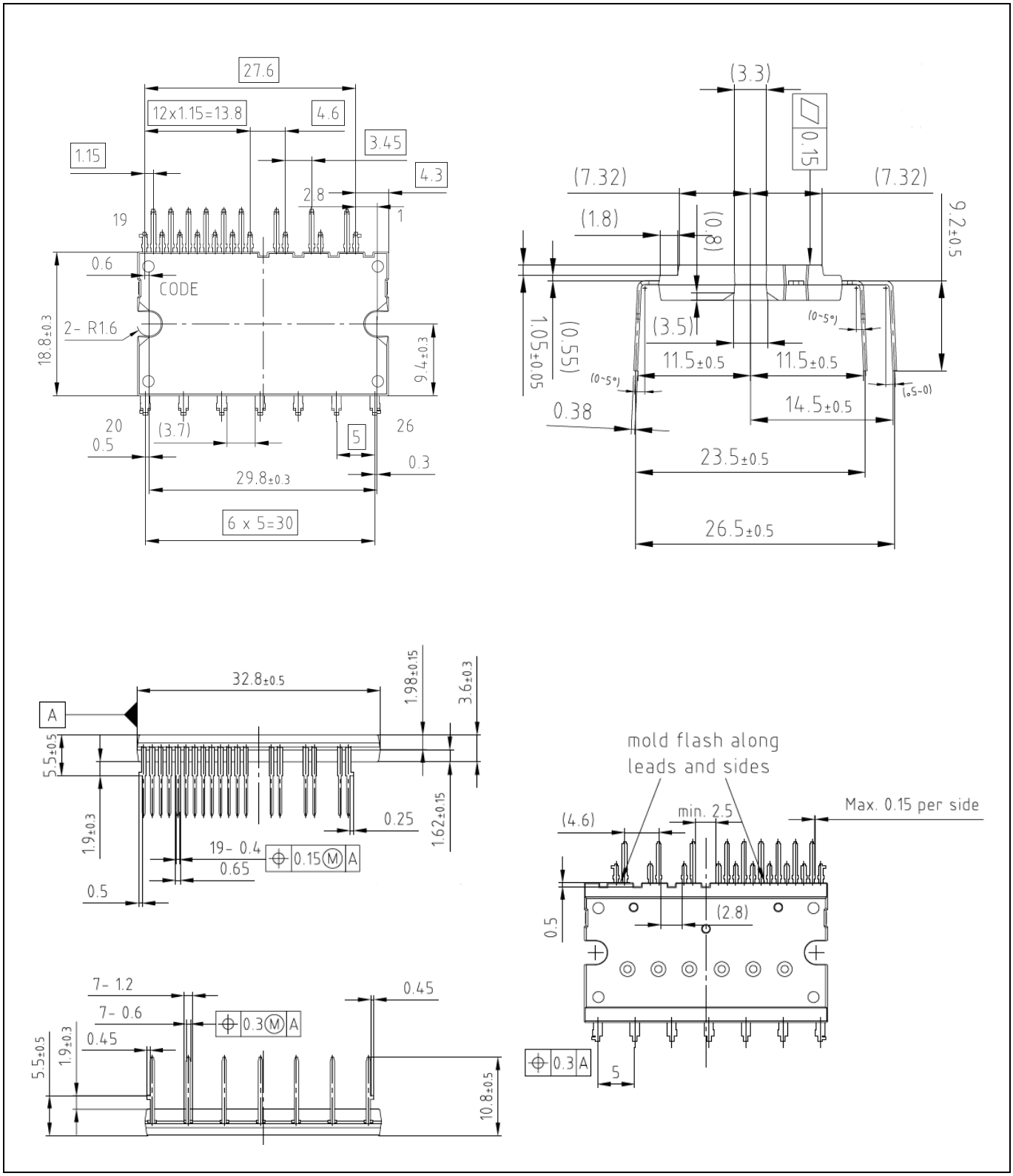


Figure 12 IM323-L6G

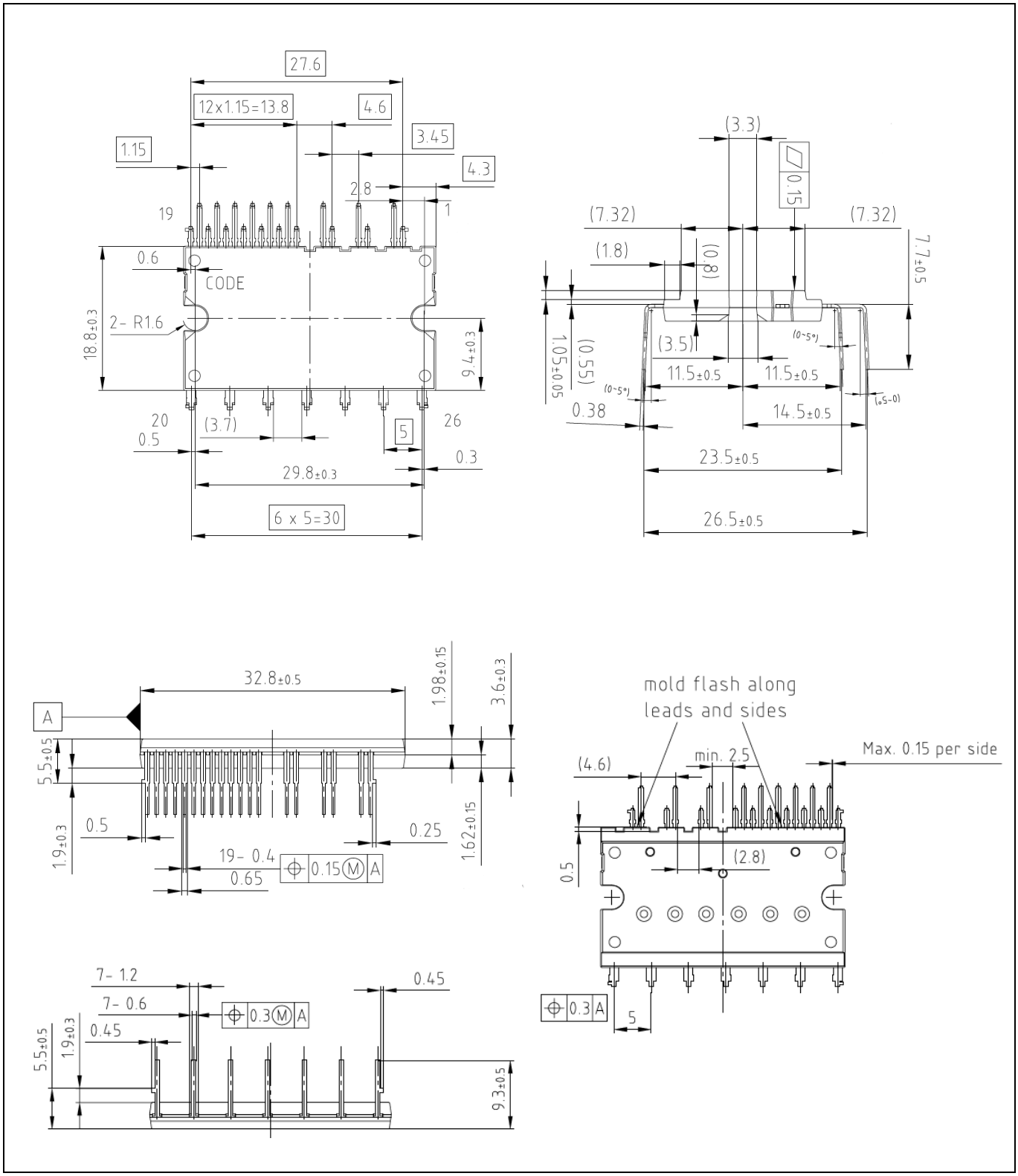


Figure 13 IM323-L6G2

Revision history

Document version	Date of release	Description of changes
V 2.0	2021-12-09	Initial release
V 2.1	2022-01-28	UL certification updated

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