

DP83TD510E Ultra Low Power 802.3cg 10Base-T1L 10M Single Pair Ethernet PHY

1 Features

- Long cable reach
 - 1700 meters+ with 1-V p2p
 - 1700 meters+ with 2.4-V p2p
- Ultra-low power
 - 45 mW for 1-V p2p mode
 - 99 mW for 2.4-V p2p mode
- Compliant to IEEE 802.3cg 10Base-T1L
- IEC 61000-4-4 EFT ±4 KV at 5 KHz, 100 KHz
- CISPR22 radiated emission class B
- External MDI terminations for intrinsic safety
- MAC interface:
 - MII mode
 - RMII master/slave mode
 - RGMII mode
 - RMII master low-power 5-MHz mode
 - RMII back-2-back mode for range extender
- Power supply
 - single supply operations from 3.3 V
 - dual supply operations for lowest power dissipation
- I/O voltages: 1.8 V, 2.5 V or 3.3 V
- Diagnostics tool kit
 - cable open and short detection
 - receiver SQI to measure cable degradation
 - active link cable diagnostics
- Clock output: 25 MHz, 50 MHz (RMII master)
- ±6-kV HBM ESD protection on MDI pins
- Operating temperature range: –40°C to 105°C
- Package: 5 mm x 5 mm, 32 pin with 0.5 mm pitch

2 Applications

- Process automation
 - Field transmitters and switches
- Building automation
 - HVAC controllers
 - Elevators and escalators
 - Fire safety
- Factory automation and control

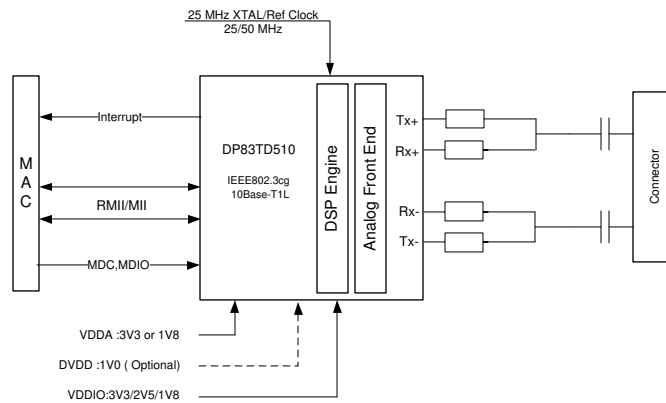
3 Description

The DP83TD510E is an ultra-low power Ethernet physical layer transceiver compliant with the IEEE 802.3cg 10Base-T1L specification. The PHY has very low noise coupled receiver architecture enabling long cable reach and very low power dissipation. The DP83TD510E has external MDI termination to support intrinsic safety requirements. It interfaces with MAC layer through MII, Reduced MII (RMII) , RGMII, and RMII low power 5-MHz master mode. It also supports RMII back-to-back mode for applications that require cable reach extension beyond 1700 meters. It supports a 25MHz reference clock output to clock other modules on the system. The DP83TD510E offers integrated cable diagnostic tools; built-in self-test, and loopback capabilities for ease of design or debug.

Device Information

| PART NUMBER ⁽¹⁾ | PACKAGE | BODY SIZE (NOM) |
|----------------------------|----------|-------------------|
| DP83TD510E | QFN (32) | 5.00 mm x 5.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



DP83TD510E Application Diagram

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An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

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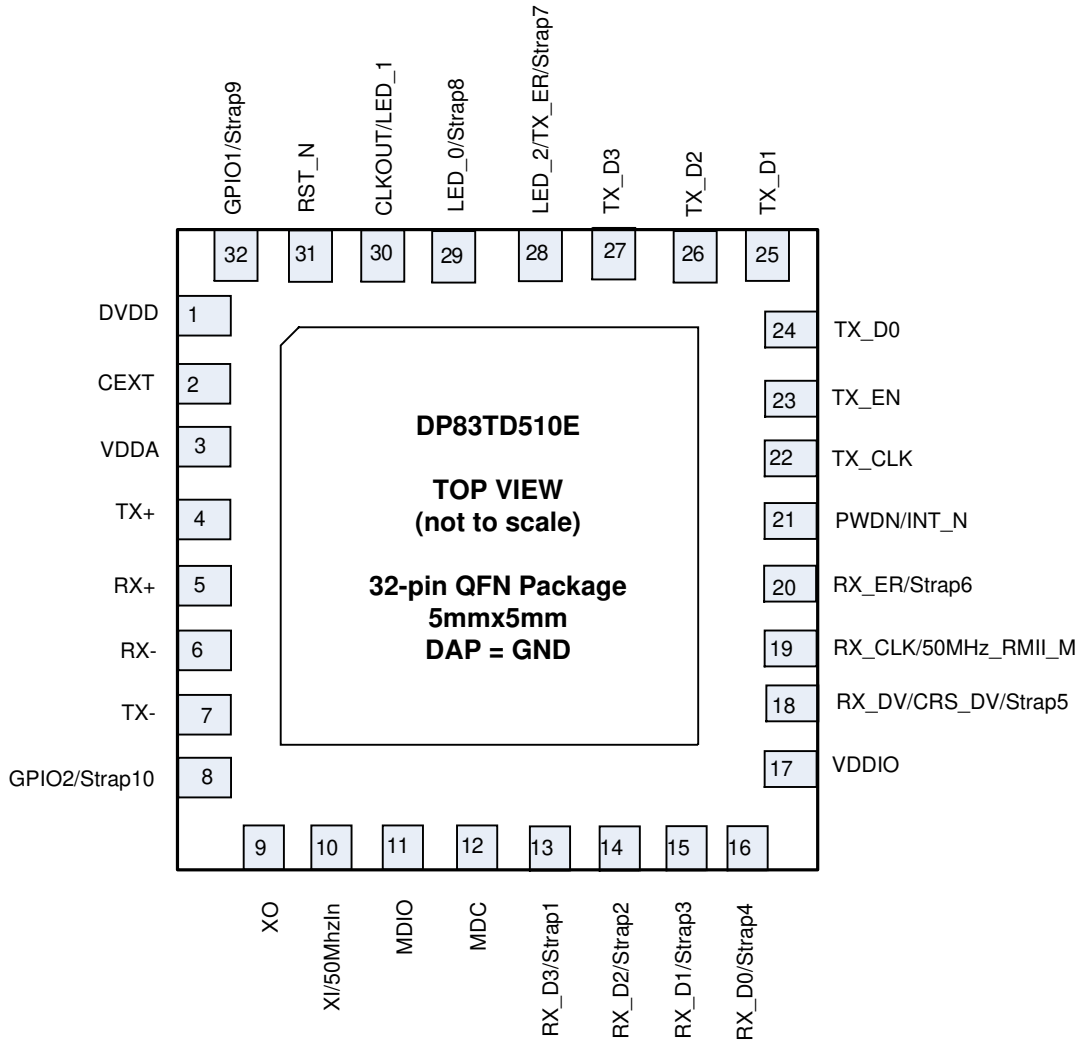
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (September 2020) to Revision B (October 2020) | Page |
|---|-------------|
| • Added long cable reach bullet to include 1700 meters+ with 1-V p2p and 1200 meters+ with 2.4-V p2p..... | 1 |
| Changes from Revision * (August 2020) to Revision A (September 2020) | Page |
| • Added DP83TD510E Registers..... | 28 |

5 Pin Configuration and Functions



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Figure 5-1. RMQ Package 32-Pin VQFN Top View

Pin Functions

| PIN | | TYPE | DESCRIPTION |
|------------------|----|-------|---|
| NAME | NO | | |
| DVDD | 1 | A | Digital supply 1.0 V <ul style="list-style-type: none"> For single-supply operation: Short this pin with CEXT (Pin 2) Optional (dual-supply operation): Connect external 1.0 V to achieve lowest power Refer to Power Connection Diagram in Application section |
| CEXT | 2 | A | External capacitor for internal LDO <ul style="list-style-type: none"> For single-supply operation: Connect 0.01- μF capacitor and short it with pin 1 For dual-supply operation, leave unconnected Refer to Power Connection Diagram in Application section |
| VDDA | 3 | A | Supply 3.3 V to support both long reach and short reach. Supply 1.8 V to support only short reach. Supplied voltage will be reflected in bit 13 of auto negotiation base page as capability to support 2.4-V p2p or 1-V p2p. 0x20E, bit 13 = 1 when 3.3 V is selected. 0x20E, bit 13 = 0 when 1.8 V is selected. Ensure the Strap7 "Reach Selection" strap is selected appropriately to request the output voltage level in the auto negotiation page. |
| TX+ | 4 | A | TX+, TX- : Differential Transmit Output (PMD): These differential outputs are configured to 2.4-V p2p or 1-V p2p signaling mode based on configuration chosen for PHY and auto negotiation with Link Partner. |
| RX+ | 5 | A | RX+, RX- : These differential inputs are automatically configured to accept 2.4-V p2p or 1-V p2p signaling mode based on configuration chosen for PHY. |
| RX- | 6 | A | |
| TX- | 7 | A | TX+, TX- : Differential Transmit Output (PMD): These differential outputs are configured to 2.4-V p2p or 1-V p2p signaling mode based on configuration chosen for PHY and auto negotiation with Link Partner. |
| GPIO2 | 8 | Strap | GPIO: This pin can be configured for multiple configuration thru register configuration. It has mandatory PU or PD strap. Refer to Straps sections for details. |
| XO | 9 | A | Crystal Output: Reference Clock output. XO pin is used for crystal only. This pin should be left floating when a CMOS-level oscillator is connected to XI. |
| XI/50MHzIn | 10 | A | Crystal / Oscillator Input Clock MII, RMII master mode: 25-MHz \pm 50 ppm-tolerance crystal or oscillator clock RMII slave mode: 50-MHz \pm 50 ppm-tolerance CMOS-level oscillator clock |
| MDIO | 11 | | Management Data I/O: Bi-directional management data signal that may be source by the management station or the PHY. This pin requires an external pull of 2.2k Ω - 4.0 k Ω . |
| MDC | 12 | | Management Data Clock: Synchronous clock to the MDIO serial management input/output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 1.75 MHz. |
| RX_D3 | 13 | Strap | Receive Data: Symbols received on the cable are decoded and presented on these pins synchronous to the rising edge of RX_CLK. They contain valid data when RX_DV is asserted. A nibble RX_D[3:0] is received in MII modes. 2-bits RX_D[1:0] is received in RMII mode. |
| RX_D2 | 14 | Strap | |
| RX_D1 | 15 | Strap | |
| RX_D0 | 16 | Strap | |
| VDDIO | 17 | Power | I/O Supply : 3.3 V/2.5 V/1.8 V. For decoupling capacitor requirements, refer to Application section of data sheet. |
| RX_DV/ CRS_DV | 18 | Strap | Receive Data Valid: This pin indicates valid data is present on the RX_D[3:0] for MII mode and on RX_D[1:0] for RMII mode. In RMII mode, this pin acts as CRS_DV and combines the RMII arrier and Receive Data Valid indications. This pin can be configured to RX_DV to enable RMII repeater mode using strap or register configuration. RGMII mode: RGMII Receive Control: RX_CTRL combines receive data valid and receive error signals. RX_DV is presented on the rising edge of RX_CLK and RX_ER on the falling edge of RX_CLK. |

| PIN | | TYPE | DESCRIPTION |
|-----------------------------|----|-------|--|
| NAME | NO | | |
| RX_CLK/ 50MHz_RMII _M | 19 | | MII Receive Clock: MII Receive Clock provides a 25-MHz reference clock for 100-Mbps speed and a 2.5-MHz reference clock for 10-Mbps speed, which is derived from the received data stream. In RMII master mode, this provides 50-MHz reference clock. In RMII slave mode, this pin is not used and remains Input/PD. RGMII Receive Clock: RGMII Receive Clock provides a 2.5-MHz reference clock for 10-Mbps speed, which is derived from the receive data stream. |
| RX_ER | 20 | Strap | Receive Error: This pin indicates that an error symbol has been detected within a received packet in both MII and RMII mode. In MII mode, RX_ER is asserted high synchronously to the rising edge of RX_CLK. In RMII mode, RX_ER is asserted high synchronously to the rising edge of the reference clock. RX_ERR is asserted high for every reception error, including errors during Idle. Unused in RGMII mode. |
| PWDN/INT | 21 | | Power Down(Default)/Interrupt: The default function of this pin is power down. Register access is required to configure this pin as an interrupt. In power down function, an active low signal on this pin places the device in power down mode. When this pin is configured as an interrupt pin, this pin is asserted low when an interrupt condition occurs. The pin has an open-drain output with a weak internal pullup (9.5 kΩ). Some applications may require an external PU resistor. |
| TX_CLK | 22 | | MII Transmit Clock: MII Transmit Clock provides a 25-MHz reference clock for 100-Mbps speed and a 2.5-MHz reference clock for 10-Mbps speed. Note that in MII mode, this clock has constant phase referenced to the reference clock. Applications requiring such constant phase may use this feature. Unused in RMII mode. RGMII Transmit Clock: The clock is sourced from the MAC layer to the PHY. When operating at 10-Mbps speed, this clock must be 2.5-MHz. |
| TX_EN | 23 | | Transmit Enable: TX_EN is presented on the rising edge of the TX_CLK. TX_EN indicates the presence of valid data inputs on TX_D[3:0] in MII mode and on TX_D[1:0] in RMII mode. TX_EN is an active high signal. RGMII Transmit Control: TX_CTRL combines transmit enable and transmit error signals. TX_EN is presented on the rising edge of TX_CLK and TX_ER on the falling edge of TX_CLK. |
| TX_D0 | 24 | | Transmit Data: In MII mode, the transmit data nibble received from the MAC is synchronous to the rising edge of TX_CLK. In RMII mode, TX_D[1:0] received from the MAC is synchronous to the rising edge of the reference clock. |
| TX_D1 | 25 | | |
| TX_D2 | 26 | | |
| TX_D3 | 27 | | |
| LED_2/ TX_ER | 28 | Strap | This pin acts as LED_2 by default. It can be configured as GPIO or TX_ER as well. The LED is ON when link is negotiated for 10M (short reach). LED remains OFF otherwise. |
| LED_0 | 29 | Strap | LED : Activity Indication LED indicates transmit and receive activity in addition to the status of the link. The LED is ON when link is good. The LED blinks when the transmitter or receiver is active. This pin can also act as GPIO using register configuration. |
| CLKOUT/ LED_1 | 30 | | This pin provides Reference CLKOUT of 25 MHz as default to clock other module on the board. The pin can be configured to act as LED_1 using strap or register configuration. The LED is ON when link is negotiated for 10M (long reach). The LED remains OFF otherwise. When configured for CLK_OUT, reference clock is not affected by reset and switches off only at IEEE Power Down. |
| RST_N | 31 | | RST_N: This pin is an active low reset input. Asserting this pin low for at least 25μs will force a reset process to occur. Initiation of reset causes strap pins to be re-scanned and resets all the internal registers of the PHY to default value. |
| GPIO1 | 32 | Strap | General Purpose Input or Output. |

Table 5-1. Internal PU/PD in various states

| Pin # | Reset State | Active State (MII Mode) | Active State (RMII Master Mode) | Active State (RMII Slave Mode) | Active State (RGMII Mode) |
|-------|-------------|--------------------------|----------------------------------|---------------------------------|---------------------------|
| 1 | A | A | A | A | A |

Table 5-1. Internal PU/PD in various states (continued)

| Pin # | Reset State | Active State (MII Mode) | Active State (RMIIMaster Mode) | Active State (RMIISlave Mode) | Active State (RGMII Mode) |
|-------|------------------------------|------------------------------|---------------------------------|--------------------------------|---------------------------|
| 2 | A | A | A | A | A |
| 3 | A | A | A | A | A |
| 4 | A | A | A | A | A |
| 5 | A | A | A | A | A |
| 6 | A | A | A | A | A |
| 7 | A | A | A | A | A |
| 8 | I,PD | I,PD | I,PD | I,PD | I,PD |
| 9 | A | A | A | A | A |
| 10 | A | A | A | A | A |
| 11 | IO | IO | IO | IO | IO |
| 12 | I | I | I | I | I |
| 13 | I,PD | O,Hi-Z | I,PD | I,PD | O,Hi-Z |
| 14 | I,PD | O,Hi-Z | I,PD | I,PD | O,Hi-Z |
| 15 | I,PD | O,Hi-Z | O,Hi-Z | O,Hi-Z | O,Hi-Z |
| 16 | I,PD | O,Hi-Z | O,Hi-Z | O,Hi-Z | O,Hi-Z |
| 17 | A | A | A | A | A |
| 18 | I,PD | O,Hi-Z | O,Hi-Z | O,Hi-Z | O,Hi-Z |
| 19 | I,PD | O,Hi-Z | O,Hi-Z | O,Hi-Z | O,Hi-Z |
| 20 | I,PD | O,Hi-Z | O,Hi-Z | O,Hi-Z | I,PD |
| 21 | I,PU-9.5KΩ/ OPEN DRAIN | I,PU-9.5KΩ/ OPEN DRAIN | I,PU-9.5KΩ/OPEN DRAIN | I,PU-9.5KΩ/OPEN DRAIN | I,PU-9.5KΩ/OPEN DRAIN |
| 22 | I,PD | O,Hi-Z | I,PD | I,PD | I,PD |
| 23 | I,PD | I,PD | I,PD | I,PD | I,PD |
| 24 | I,PD | I,PD | I,PD | I,PD | I,PD |
| 25 | I,PD | I,PD | I,PD | I,PD | I,PD |
| 26 | I,PD | I,PD | I,PD | I,PD | I,PD |
| 27 | I,PD | I,PD | I,PD | I,PD | I,PD |
| 28 | I,PD | O,Hi-Z | O,Hi-Z | O,Hi-Z | O,Hi-Z |
| 29 | I,PD | O,Hi-Z | O,Hi-Z | O,Hi-Z | O,Hi-Z |
| 30 | I,PD(Only at POR) | O,Hi-Z | O,Hi-Z | O,Hi-Z | O,Hi-Z |
| 31 | I,PU | I,PU | I,PU | I,PU | I,PU |
| 32 | I,PD | O,Hi-Z | O,Hi-Z | O,Hi-Z | O,Hi-Z |

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| PARAMETER | | MIN | MAX | UNIT |
|----------------|-------------------------------------|------|-------------|------|
| Supply voltage | DVDD 1.0 | -0.3 | 1.4 | V |
| | VDDA 1.8 | -0.3 | 4 | V |
| | VDDA 3.3 | -0.3 | 4 | V |
| | VDDIO (3.3) | -0.3 | 4 | V |
| | VDDIO (2.5) | -0.3 | 3 | V |
| | VDDIO (1.8) | -0.3 | 2.1 | V |
| Pins | MDI (Tx+, Tx-, Rx+, Rx-) | -0.3 | 4 | V |
| Pins | MAC Interface, MDIO, MDC, GPIO, LED | -0.3 | VDDIO + 0.3 | V |
| Pins | INT/PWDN, RESET | -0.3 | VDDIO + 0.3 | V |
| Pins | XI Oscillator Input | -0.3 | VDDIO+0.3 | V |

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| Parameter | | | | VALUE | UNIT |
|--------------------|--------------------------------|--|---------------------|---------|------|
| V _(ESD) | V(ESD) Electrostatic discharge | Human-body model (HBM), perANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | All pins except MDI | +/-2000 | V |
| V _(ESD) | V(ESD) Electrostatic discharge | Human-body model (HBM), perANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | MDI pins | +/-6000 | V |
| V _(ESD) | V(ESD) Electrostatic discharge | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | All Pins | +/-500 | V |

- (1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500 V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250 V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| Parameter | | MIN | NOM | MAX | UNIT |
|----------------|---|------------|-------|------------|------|
| DVDD 1.0 | Digital Supply | 0.90 | 1.0 | 1.1 | V |
| VDDA 1.8 | Analog Supply | 1.62 | 1.8 | 1.98 | V |
| VDDA 3.3 | Analog Supply | 3.0 | 3.3 | 3.6 | V |
| VDDIO | Digital Supply Voltage, 1.8V operation | 1.62 | 1.8 | 1.98 | V |
| | Digital Supply Voltage, 2.5V operation | 2.25 | 2.5 | 2.75 | |
| | Digital Supply Voltage, 3.3V operation | 3.0 | 3.3 | 3.6 | |
| T _A | Operating Ambient Temperature | -40 | | 105 | °C |
| Pins | TX_D[0:3],RX_D[0:3], TX_CLK, RX_CLK, TX_EN, RX_DV, RX_ER, MDIO, MDC, LED0, LED1, LED2 | VDDIO-10 % | VDDIO | VDDIO +10% | V |
| Pins | INT/PWDN, RESET_N | VDDIO-10 % | VDDIO | VDDIO +10% | V |
| Pins | XI Oscillator Input | VDDIO-10 % | VDDIO | VDDIO +10% | V |

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over operating free-air temperature range (unless otherwise noted)

| Parameter | | MIN | NOM | MAX | UNIT |
|-----------|------|---------------|-------|---------------|------|
| Pins | GPIO | VDDIO-10 % | VDDIO | VDDIO +10% | V |

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6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | 32PIN QFN | UNIT |
|-------------------------------|--|-----------|------|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 52 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 42 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 31.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 2.1 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 31.4 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 11.9 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------------------------|--|------|------|------|------|
| IEEE Tx CONFORMANCE (10BaseT1L External Terminations) | | | | | | |
| 1V p2p | Vod : Output Differential Voltage | | 0.85 | 1.0 | 1.05 | V |
| 2.4-V p2p | Vod : Output Differential Voltage | | 2.04 | 2.4 | 2.56 | V |
| POWER CONSUMPTION (Dual Analog Supply, 1-V p2p mode) | | | | | | |
| | DVDD1.0 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 5 | | mA |
| | AVDD1.8 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 18 | | mA |
| | DVDD1.0 | Reset | | 3 | | mA |
| | AVDD1.8 | Reset | | 5 | | mA |
| POWER CONSUMPTION (Dual Analog Supply, 2.4V p2p mode) | | | | | | |
| | DVDD1.0 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 5 | | mA |
| | AVDD3.3 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 26.5 | | mA |
| Power Consumption VDDIO (MII Interface) | | | | | | |
| | VDDIO1.8 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 4 | | mA |
| | VDDIO2.5 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 5 | | mA |
| | VDDIO3.3 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 6 | | mA |
| Power Consumption VDDIO (RMII Master Interface) | | | | | | |
| | VDDIO1.8 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 8.5 | | mA |
| | VDDIO2.5 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 12 | | mA |
| | VDDIO3.3 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 16 | | mA |

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--------------------------------------|--|-----|-----|-----|------|
| Power Consumption VDDIO (RMII Slave Interface) | | | | | | |
| | VDDIO1.8 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 4 | | mA |
| | VDDIO2.5 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 5 | | mA |
| | VDDIO3.3 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 6 | | mA |
| Power Consumption VDDIO (RMII Master 5 MHz) | | | | | | |
| | VDDIO1.8 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 4 | | mA |
| | VDDIO2.5 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 5 | | mA |
| | VDDIO3.3 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 6 | | mA |
| Power Consumption VDDIO (RGMII Interface) | | | | | | |
| | VDDIO1.8 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 4 | | mA |
| | VDDIO2.5 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 5 | | mA |
| | VDDIO3.3 | 100% Traffic, Random Size : 64 to 1512 Bytes, Random Content | | 6 | | mA |
| BOOTSTRAP DC CHARACTERISTICS (2 Level) | | | | | | |
| V _{IH_3v3} | High Level Bootstrap Threshold : 3V3 | | 1.3 | | | V |
| V _{IL_3v3} | Low Level Bootstrap Threshold : 3V3 | | | | 0.6 | V |
| V _{IH_2v5} | High Level Bootstrap Threshold: 2V5 | | 1.3 | | | V |
| V _{IL_2v5} | Low Level Bootstrap Threshold : 2V5 | | | | 0.6 | V |
| V _{IH_1v8} | High Level Bootstrap Threshold:1V8 | | 1.3 | | | V |
| V _{IL_1v8} | Low Level Bootstrap Threshold :1V8 | | | | 0.6 | V |

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over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|---|--|----------------|----------------|------|------|
| IO CHARACTERISTICS | | | | | | |
| V _{IH} | High Level Input Voltage | VDDIO = 3.3V ±10% | 2 | | | V |
| V _{IL} | Low Level Input Voltage | VDDIO = 3.3V ±10% | | | 0.8 | V |
| V _{OH} | High Level Output Voltage | I _{OH} = -2mA, VDDIO = 3.3V ±10% | 2.4 | | | V |
| V _{OL} | Low Level Output Voltage | I _{OL} = 2mA, VDDIO = 3.3V ±10% | | | 0.4 | V |
| V _{IH} | High Level Input Voltage | VDDIO = 2.5V ±10% | 1.7 | | | V |
| V _{IL} | Low Level Input Voltage | VDDIO = 2.5V ±10% | | | 0.7 | V |
| V _{OH} | High Level Output Voltage | I _{OH} = -2mA, VDDIO = 2.5V ±10% | 2 | | | V |
| V _{OL} | Low Level Output Voltage | I _{OL} = 2mA, VDDIO = 2.5V ±10% | | | 0.4 | V |
| V _{IH} | High Level Input Voltage | VDDIO = 1.8V ±10% | 0.65*VD DIO | | | V |
| V _{IL} | Low Level Input Voltage | VDDIO = 1.8V ±10% | | 0.35*VD DIO | | V |
| V _{OH} | High Level Output Voltage | I _{OH} = -2mA, VDDIO = 1.8V ±10% | VDDIO-0 .45 | | | V |
| V _{OL} | Low Level Output Voltage | I _{OL} = 2mA, VDDIO = 1.8V ±10% | | | 0.45 | V |
| I _{IH} | Input High Current | T _A = -40°C to 105°C, VIN=VDDIO | | 15 | | μA |
| I _{IL} | Input Low Current | T _A = -40°C to 105°C, VIN=GND | | 15 | | μA |
| R _{pulldn} | Internal Pull Down Resistor | | | 9 | | kΩ |
| R _{pullup} | Internal Pull Up Resistor | | | 9 | | kΩ |
| XI V _{IH} | High Level Input Voltage | | 1.2 | | | V |
| XI V _{IL} | Low Level Input Voltage | | | | 0.6 | V |
| C _{IN} | Input Capacitance XI | | | 1 | | pF |
| C _{IN} | Input Capacitance INPUT PINS (TX_D[3:0], TX_EN, TX_CLK, MDC) | | | 5 | | pF |
| C _{OUT} | Output Capacitance XO | | | 1 | | pF |
| C _{OUT} | Output Capacitance OUTPUT PINS | | | 5 | | pF |
| R _{series} | Integrated MAC Series Termination Resistor | RX_D[3:0], RX_ER, RX_DV, RX_CLK | | 50 | | Ω |
| | LED drive strength | | | 8 | | mA |

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6.6 Timing Requirements

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|--|--|---------------------------------------|------|-----|-----|------|
| POWER-UP TIMING (Single and Dual supply mode) | | | | | | |
| | Supply ramp rate: For all supplies (DVDD, VDDA, VDDIO) | (20% to 80%) | 0.2 | | 40 | ms |
| | Supply ramp delay offset: For all supplies (DVDD, VDDA, VDDIO) | First Supply ramp to last supply ramp | | | 200 | ms |
| T1 | Last Supply power up to RESET_N High | | | | 60 | ms |
| T2 | Powerup to SMI ready: Post power-up stabilization time prior to MDC preamble for register access | | | | 60 | ms |
| T3 | Powerup to Strap latchin: Hardware configuration pins transition to output drivers | | | | 60 | ms |
| | Pedestal Voltage on DVDD, VDDA, VDDIO before Power Ramp | | | | 0.3 | V |
| RESET TIMING | | | | | | |
| T1 | Reset to SMI ready: Post reset stabilization time prior to MDC preamble for register access | | 30 | | | us |
| T3 | RESET PULSE Width: Minimum Reset pulse width to be able to reset | | 10 | | | us |
| T5 | Reset to MAC clock (MII RX_CLK) | | | 995 | | us |
| MII 10M Timings | | | | | | |
| 10M | TX_CLK High / Low Time | | 190 | 200 | 210 | ns |
| | TX_D[3:0], TX_ER, TX_EN Setup to TX_CLK | | 25 | | | ns |
| | TX_D[3:0], TX_ER, TX_EN Hold from TX_CLK | | 0 | | | ns |
| | RX_CLK High / Low Time | | 160 | 200 | 240 | ns |
| | RX_D[3:0], RX_ER, RX_DV Delay from RX_CLK rising | | 100 | | 300 | ns |
| RGMII OUTPUT TIMING (10M) | | | | | | |
| T _{skewT} | Data to Clock Output Skew (Non-Delay Mode) | 5 pF Load | -2 | | 2 | ns |
| T _{skewR} | Data to Clock Output Setup (Integrated Delay) | | 30 | | | ns |
| T _{skewR} | Data to Clock Output Hold (Integrated Delay) | | 30 | | | ns |
| T _{cyc} | Clock Cycle Duration | | -360 | 400 | 440 | ns |
| | Duty Cycle | | 45 | 50 | 55 | % |
| | Rise / Fall Time (20% to 80%) | | | | 3 | ns |
| RGMII INPUT TIMING (10M) | | | | | | |
| T _{skewR} | TX data to clock input skew (Integrated Delay Mode) | | -4 | | 4 | ns |
| T _{setupR} | TX data to clock input setup (Non-Delay Mode) | | 40 | | | ns |
| T _{holdR} | TX clock to data input hold (Non-Delay Mode) | | 40 | | | ns |
| RMII MASTER TIMING | | | | | | |
| | RMII Master Clock Period | | | 20 | | ns |
| | RMII Master Clock Duty Cycle | | 35 | | 65 | % |
| | TX_D[1:0], TX_ER, TX_EN Setup to RMII Master Clock | 25 pF Load | 4 | | | ns |
| | TX_D[1:0], TX_ER, TX_EN Hold from RMII Master Clock | 25 pF Load | 2 | | | ns |
| | RX_D[1:0], RX_ER, CRS_DV Delay from RMII Master Clock rising edge | 25 pF Load | 4 | 10 | 14 | ns |
| RMII SLAVE TIMING | | | | | | |
| | Input Reference Clock Period | | | 20 | | ns |
| | Reference Clock Duty Cycle | | 35 | | 65 | % |
| | TX_D[1:0], TX_ER, TX_EN Setup to XI Clock rising | | 4 | | | ns |
| | TX_D[1:0], TX_ER, TX_EN Hold from XI Clock rising | | 2 | | | ns |

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| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|-----------------|------|-----|------|------|
| | RX_D[1:0], RX_ER, CRS_DV Delay from XI Clock rising | | 4 | | 14 | ns |
| RMII Master Timing (5 MHz) | | | | | | |
| | Frequency | | | 5 | | MHz |
| | Duty Cycle | | 40 | | 60 | % |
| | TX_D[3:0], TX_ER, TX_EN setup to Master Clock | | 10 | | | ns |
| | TX_D[3:0], TX_ER, TX_EN from Master Clock | | 10 | | | ns |
| | RX_D[3:0], RX_ER, RX_DV Delay from 5 MHz Clock | | 50 | 100 | 150 | ns |
| SMI TIMING | | | | | | |
| T1 | MDC to MDIO (Output) Delay Time | | 0 | | 10 | ns |
| T2 | MDIO (Input) to MDC Setup Time | | 10 | | | ns |
| T3 | MDIO (Input) to MDC Hold Time | | 10 | | | ns |
| T4 | MDC Frequency | | | 1 | 1.75 | MHz |
| OUTPUT CLOCK TIMING (25MHz clockout) | | | | | | |
| | Frequency (PPM) | | -100 | | 100 | - |
| | Duty Cycle | | 40 | | 60 | % |
| | Rise Time | | | | 5000 | ps |
| | Fall Time | | | | 5000 | ps |
| | Frequency | | | 25 | | MHz |
| Output Clock 50 MHz timing | | | | | | |
| | Frequency (PPM) | | -50 | | 50 | ppm |
| | Duty Cycle | | 35 | | 65 | % |
| | Rise time | | | | 5000 | ps |
| | Fall Time | | | | 5000 | ps |
| 25MHz INPUT CLOCK tolerance | | | | | | |
| | Frequency Tolerance | | -100 | | +100 | ppm |
| | Rise / Fall Time (10%-90%) | | | | 8 | ns |
| | Duty Cycle | | 40 | | 60 | % |
| 50MHz Input Clock Tolerance | | | | | | |
| | Frequency Tolerance | | -100 | | +100 | ppm |
| | Rise / Fall Time (10%-90%) | | | | 8 | ns |
| | Duty Cycle | | 40 | | 60 | % |

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6.7 Timing Diagrams

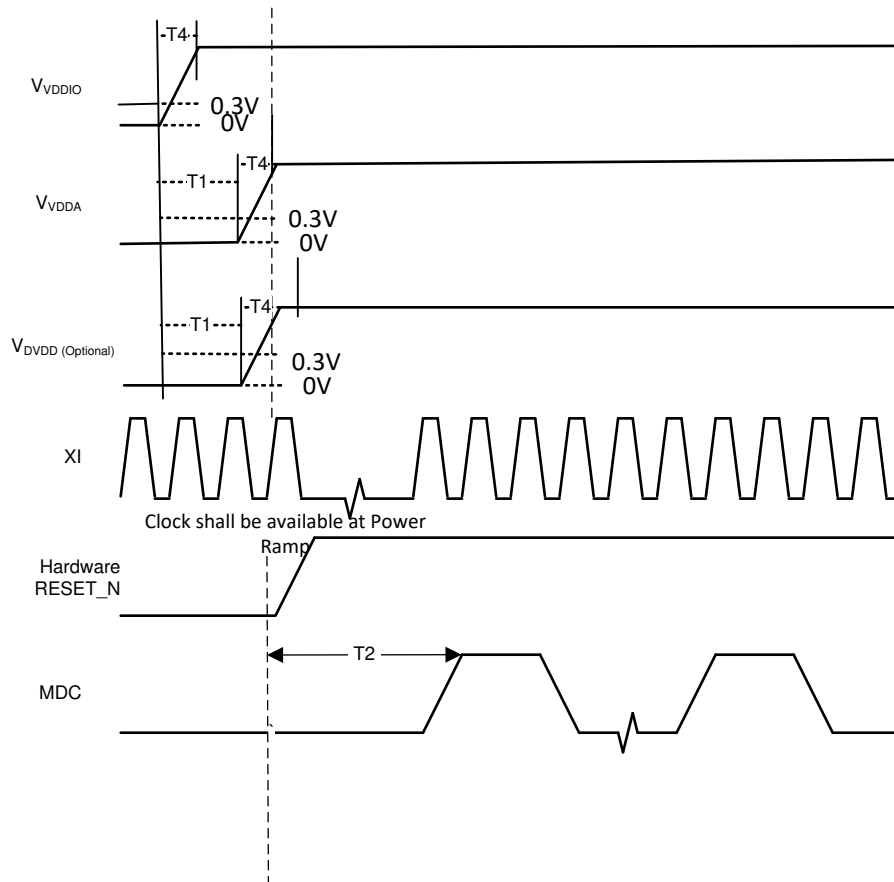


Figure 6-1. Power-Up Timing

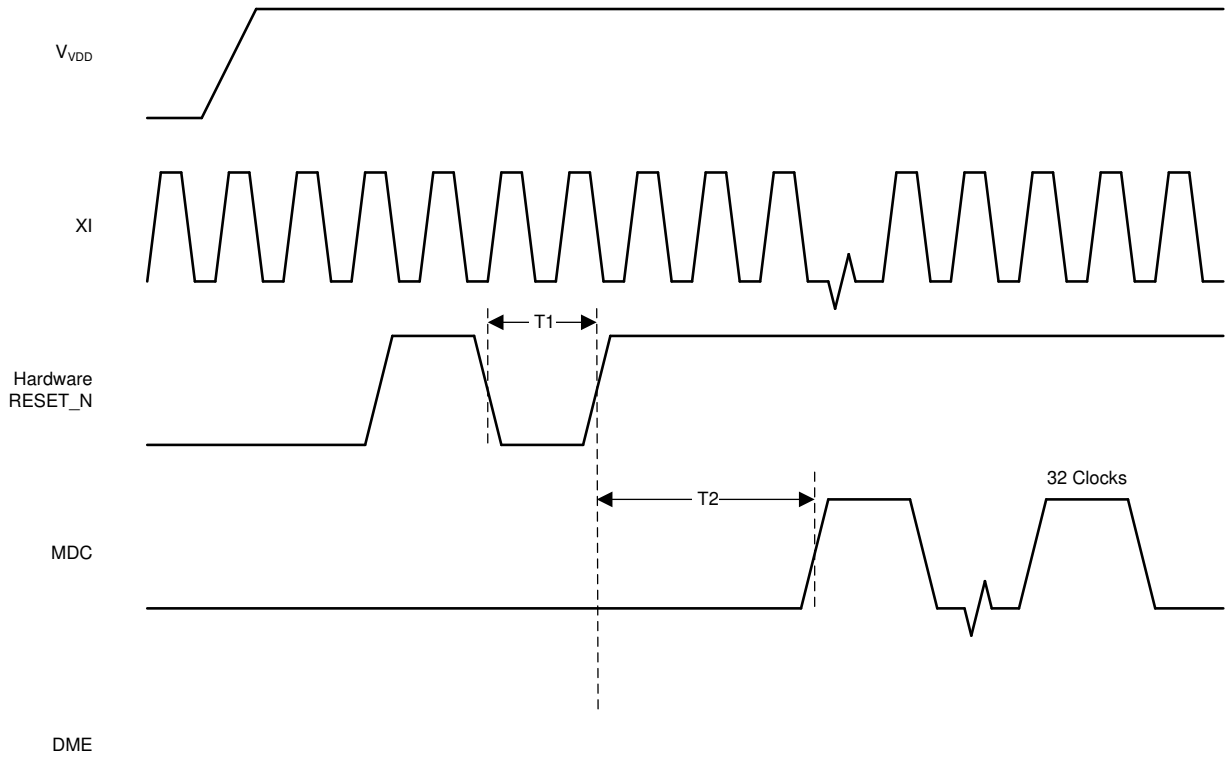


Figure 6-2. Reset Timing

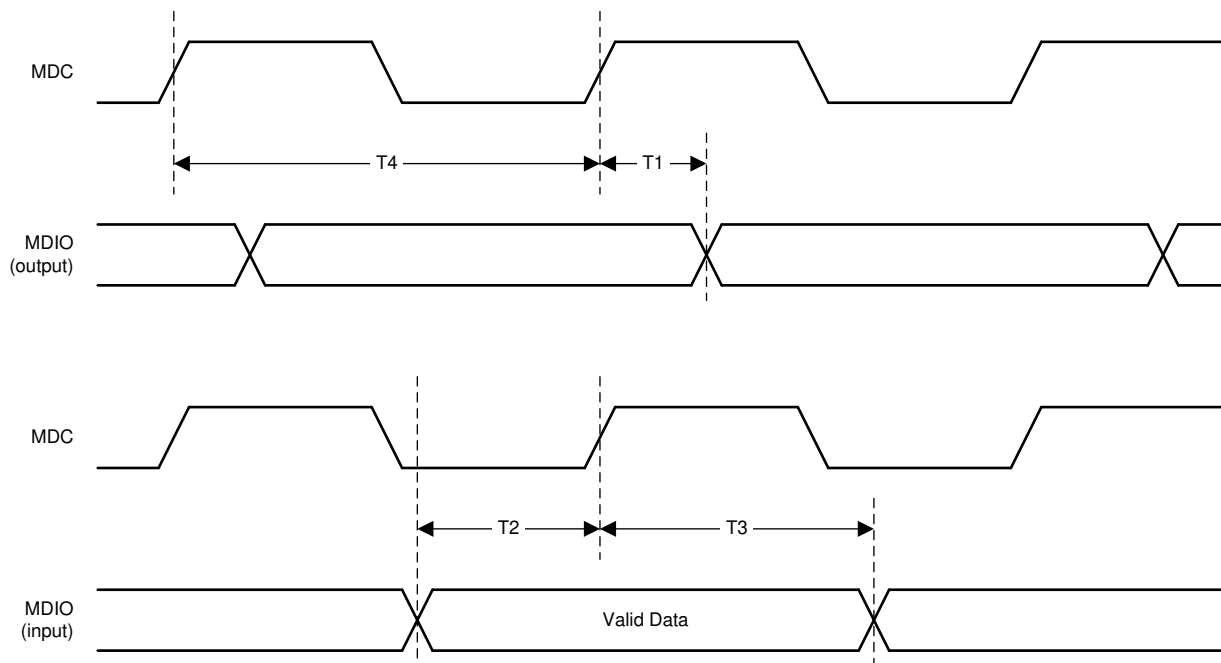


Figure 6-3. Serial Management Timing

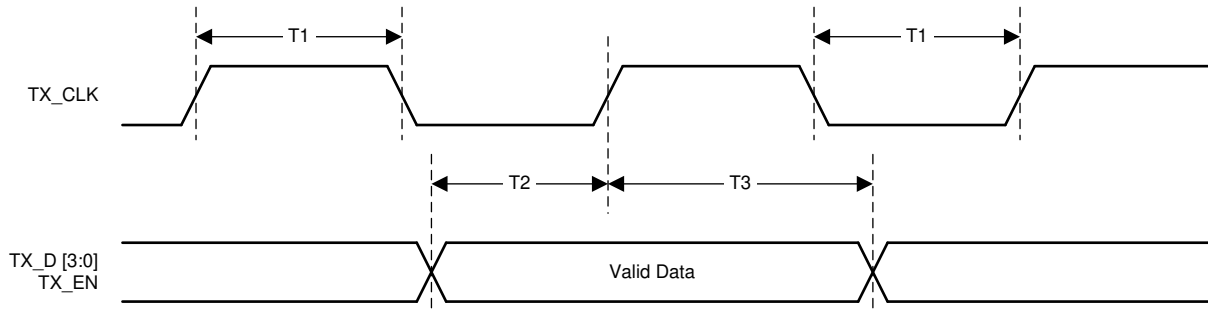


Figure 6-4. 10-Mbps MII Transmit Timing

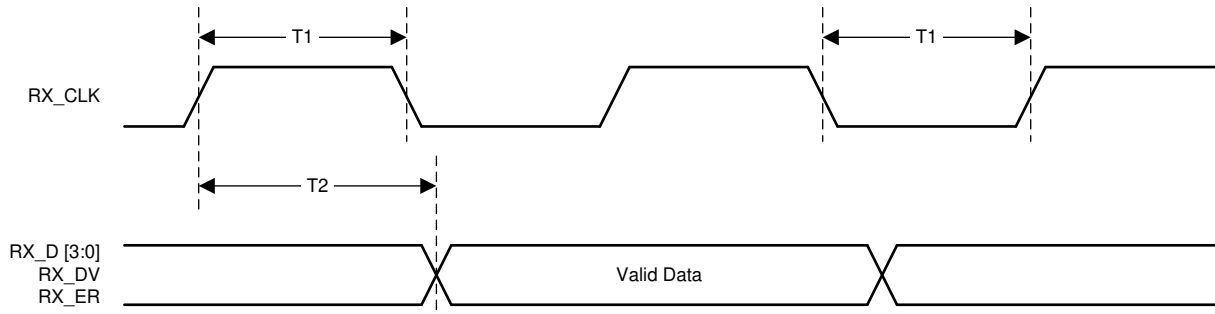


Figure 6-5. 10-Mbps MII Receive Timing

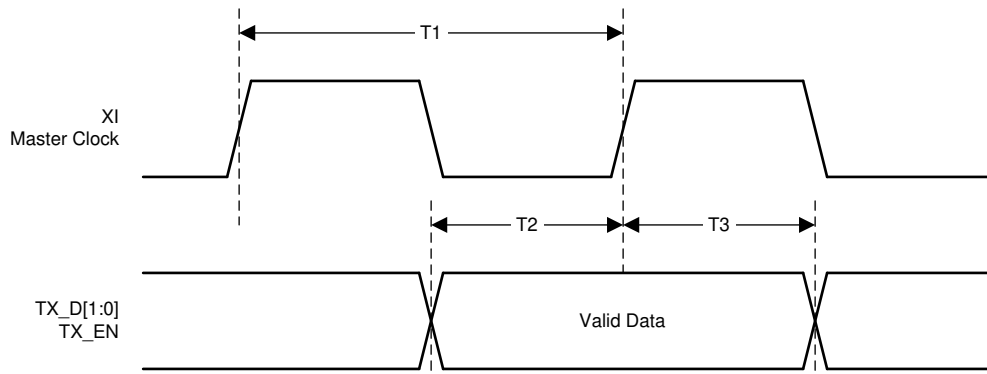


Figure 6-6. RMII Transmit Timing

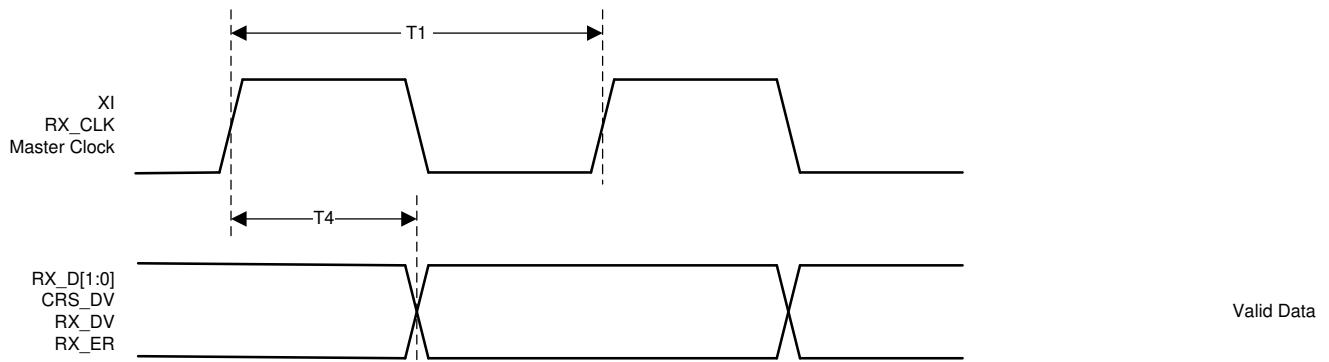


Figure 6-7. RMII Receive Timing

7 Detailed Description

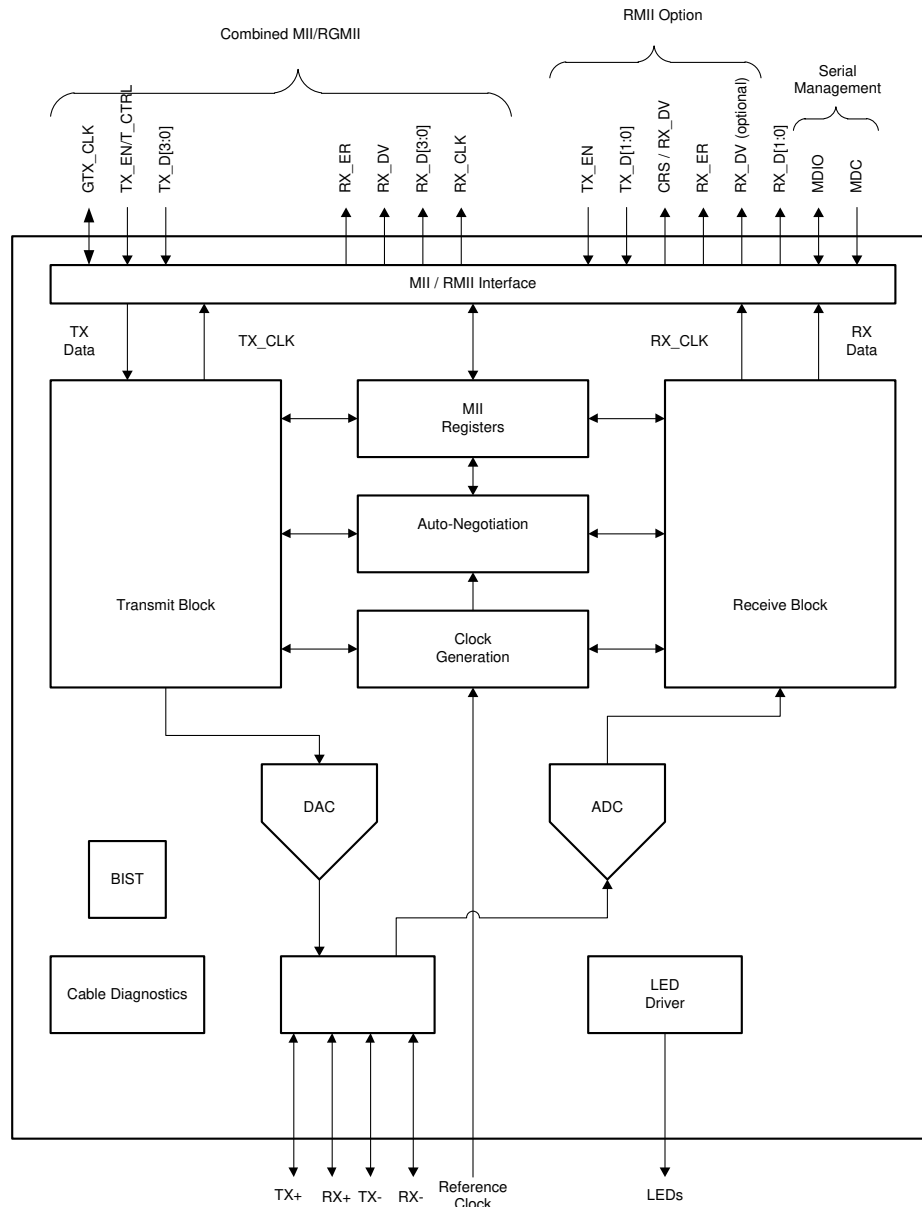
7.1 Overview

The DP83TD510E is a physical-layer transceiver compliant to IEEE 802.3cg 10BaseT1L standards. The PHY use low noise coupled signal processing receiver architecture to offer longer cable reach along with ultra-low power consumption. The device supports both 2.4-V p2p and 1-V p2p output voltage as defined by IEEE 802.3cg 10Base-T1L specifications. It supports multiple MAC interface (MII, Reduced Media Independent Interface (RMII), RGMII and low power Reduced MII) for direct connection to Media Access Controller (MAC). The device also supports back-to-back RMII mode in unmanaged mode to provide range extension and repeater functionality.

The device is designed to operate from a single 3.3-V power supply and has integrated LDO to provide the voltage rails required for internal blocks. The device has an option to feed digital power externally to achieve lowest power consumption. The device allows I/O voltage interfaces for 3.3 V, 2.5 V or 1.8 V. Automatic supply configuration within the DP83TD510E allows for any combination of VDDIO supply without the need for additional configuration settings.

The DP83TD510E Diagnostic Tool includes TDR (Time Domain Reflectometry), ALCD (Active Link Cable Diagnostics), SQI (Signal Quality Indicator), multiple Loopbacks and Integrated PRBS Packet Generator to ease debugging during development and detecting faulty conditions in field.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Auto-Negotiation (Speed Selection)

Auto-Negotiation provides a mechanism for exchanging configuration information between the two ends of a link segment. The DP83TD510E supports auto-negotiation for Low Speed Modes (LSM) as defined in IEEE 802.3cg specification for 10BaseT1L. Auto-negotiation ensures that the highest common speed is selected based on the advertised abilities of the link partner and the local device.

7.3.2 RMII Repeater Mode

The DP83TD510E provides an option to enable repeater mode functionality to extend the cable reach. Two DP83TD510E can be connected in back to back mode without any external configuration. A hardware strap is provided to configure the CRS_DV pin of RMII interface to RX_DV pin for back to back operation. Refer to [Figure 7-1](#) for the RMII pin connection to enable repeater mode on the DP83TD510E.

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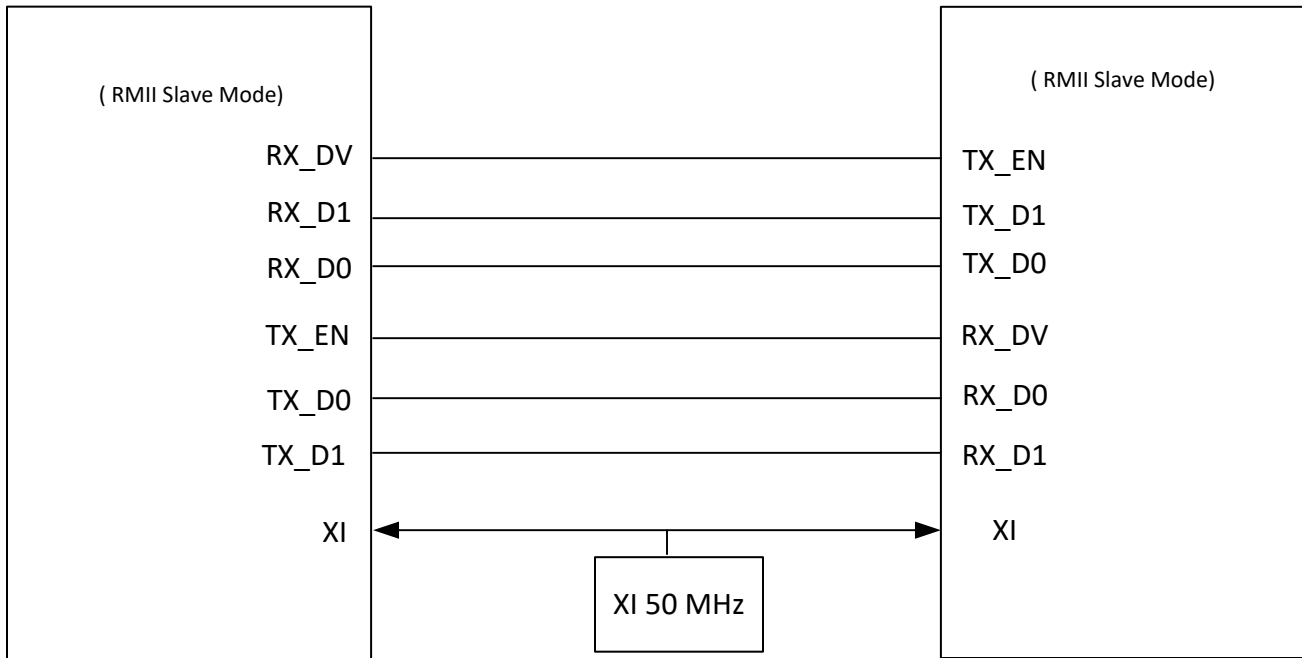


Figure 7-1. RMI Repeater Mode

7.3.3 Clock Output

The DP83TD510E has several clock output configuration options. An external crystal or CMOS-level oscillator provides the stimulus for the internal PHY reference clock. The local reference clock acts as the central source for all clocking within the device.

All clock configuration options are enabled using the IO MUX GPIO Control Register **TBD**

Clock options supported by the DP83TD510E include:

- MAC IF clock
- XI clock
- Free-running clock
- Recovered clock

7.3.4 Media Independent Interface (MII)

The Media Independent Interface is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC. The MII is fully compliant with IEEE 802.3-2002 clause 22.

The MII signals are summarized in [Table 7-1](#).

Table 7-1. MII Signals

| FUNCTION | PINS |
|------------------------------|-----------|
| Data Signals | TX_D[3:0] |
| | RX_D[3:0] |
| Transmit and Receive Signals | TX_EN |
| | RX_DV |

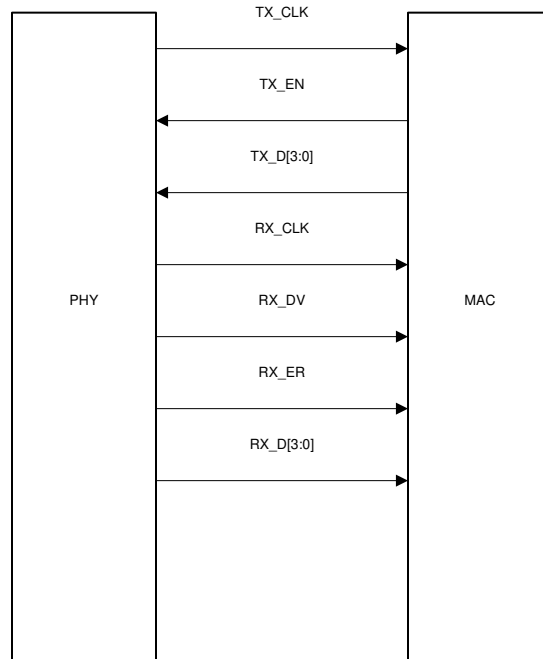


Figure 7-2. MII Signaling

Additionally, the MII interface includes the carrier sense signal (CRS), as well as a collision detect signal (COL). The CRS signal asserts to indicate the reception or transmission of data. The COL signal asserts as an indication of a collision which can occur during half-duplex mode when both transmit and receive operations occur simultaneously.

7.3.5 Reduced Media Independent Interface (RMII)

The DP83TD510E incorporates the Reduced Media Independent Interface (RMII) as specified in the RMII specification v1.2. The purpose of this interface is to provide a reduced pin count alternative to the IEEE 802.3 MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but can be implemented in the absence of an MII. The DP83TD510E offers two types of RMII operations: RMII Slave and RMII Master. In RMII Master operation, the DP83TD510E operates off of either a 25-MHz CMOS-level oscillator connected to XI pin or a 25-MHz crystal connected across XI and XO pins. A 50-MHz output clock referenced from DP83TD510E can be connected to the MAC. In RMII Slave operation, the DP83TD510E operates off of a 50-MHz CMOS-level oscillator connected to the XI pin and shares the same clock as the MAC. Alternatively, in RMII Slave mode, the PHY can run from a 50-MHz clock provided by the Host MAC.

The RMII specification has the following characteristics:

- Single clock reference sourced from the MAC to PHY (or from an external source)
- Independent 2-bit wide transmit and receive data paths
- Usage of CMOS signal levels, the same levels as the MII interface

In this mode, data transfers are two bits for every clock cycle using the internal 50-MHz reference clock for both transmit and receive paths.

The RMII signals are summarized in [Table 7-2](#).

Table 7-2. RMII Signals

| FUNCTION | PINS |
|-------------------------|-----------|
| Receive Data Lines | TX_D[1:0] |
| Transmit Data Lines | RX_D[1:0] |
| Receive Control Signal | TX_EN |
| Transmit Control Signal | CRS_DV |

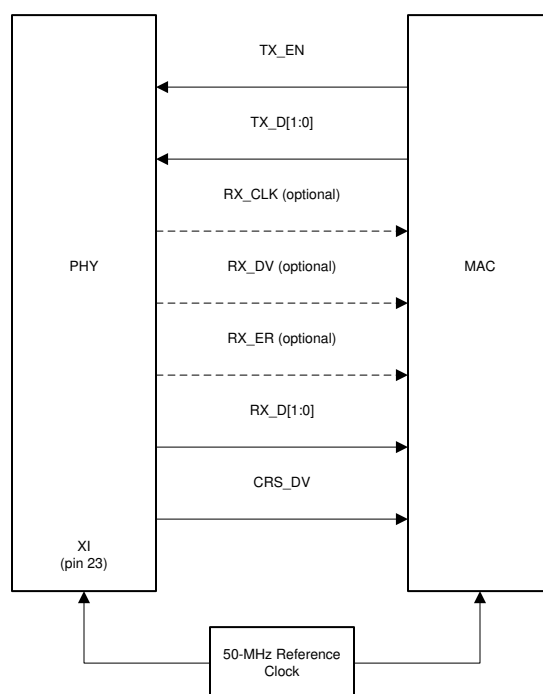


Figure 7-3. RMII Slave Signaling

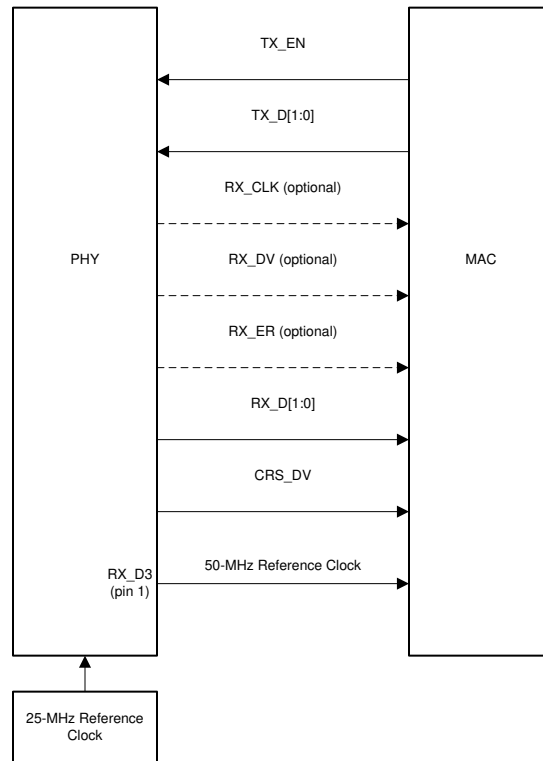


Figure 7-4. RMII Master Signaling

Data on TX_D[1:0] are latched at the PHY with reference to the clock edges on the XI pin. Data on RX_D[1:0] are latched at the MAC with reference to the same clock edges on the XI pin.

In addition, CRX_DV can be configured as RX_DV signal. It allows a simpler method of recovering receive data without the need to separate RX_DV from the CRS_DV indication.

7.3.6 RMII Low Power 5-MHz Mode

DP83TD510E supports a new MAC Mode called RMII Master Low Power Mode. The interface is similar to the RMII master mode but runs at 5 MHz resulting in power dissipation savings. DP83TD510E offers 5-MHz clock output and data is aligned to this clock. An application can use the same pin map as RMII for this mode.

7.3.7 RGMII Interface

DP83TD510E offers RGMII mode which runs at 2.5 MHz. The timing specifications are relaxed compared to RGMII at 125 MHz. Refer to timing sections on timing specifications for this mode.

7.3.8 Serial Management Interface

The Serial Management Interface provides access to the DP83TD510E internal register space for status information and configuration. The SMI is compatible with IEEE 802.3 clause 22 and clause 45. The implemented register set consists of the registers required by IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83TD510E.

The SMI includes the management clock (MDC) and the management input/output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 25 MHz. MDC is not expected to be continuous and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. The MDIO pin requires a pullup resistor (2.2 kΩ) which pulls MDIO high during IDLE and turnaround.

Up to 16 PHYs can share a common SMI bus. To distinguish between the PHYs, during power up or hardware reset, the DP83TD510E latches the Phy_Address[3:0] configuration pins to determine its address.

The management entity must not start an SMI transaction in the first cycle after power up or hardware reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after reset is de-asserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern ensures that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of turnaround. The addressed DP83TD510E drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83TD510E, thus eliminating the requirement for MDIO Turnaround. The turnaround time is filled by the management entity by inserting <10>.

Table 7-3. SMI Protocol

| SMI PROTOCOL | <idle><start><op code><PHY address><reg addr><turnaround><data><idle> |
|-----------------|---|
| Read Operation | <idle><01><10><AAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle> |
| Write Operation | <idle><01><01><AAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle> |

7.3.9 Loopback Modes

There are several loopback options within the DP83TD510E that test and verify various functional blocks within the PHY. Enabling loopback modes allow for in-circuit testing of the digital and analog data paths. The DP83TD510E may be configured to any one of the Near-End Loopback modes or to the Far-End (reverse) Loopback mode. MII Loopback is configured using the Control Register (BMCR, address TBD). All other loopback modes are enabled using the BIST Control Register (BISCR, address TBD).

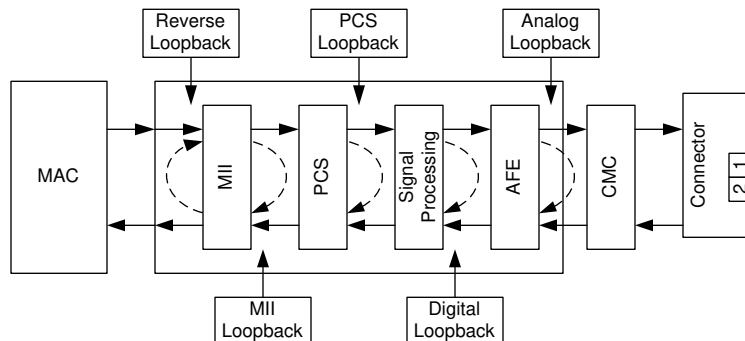


Figure 7-5. Loopback Test Modes

7.3.9.1 MII Loopback

MII Loopback is the shallowest loop through the PHY. It is a useful test mode to validate communications between the MAC and the PHY. When in MII Loopback, data transmitted from a connected MAC on the TX path is internally looped back in the DP83TD510E to the RX pins where it can be checked by the MAC.

7.3.9.2 PCS Loopback

PCS Loopback occurs in the PCS layer of the PHY. No signal processing is performed when using PCS Loopback.

7.3.9.3 Digital Loopback

Digital Loopback includes the entire digital transmit and receive paths. Data is looped back prior to the analog circuitry.

Digital Loopback is enabled by setting bit[2] in the BISCR.

7.3.9.4 Analog Loopback

Analog Signals can be looped back after the analog front-end. Details: TBD.

7.3.9.5 Far-End (Reverse) Loopback

Far-End (Reverse) loopback is a special test mode to allow PHY testing with a link partner. In this mode, data that is received from the link partner passes through the PHY's receiver, is looped back at the MAC interface and then transmitted back to the link partner. While in Reverse Loopback mode, all data signals that come from the MAC are ignored.

7.3.10 BIST Configurations

The DP83TD510E incorporates an internal PRBS Built-in Self-Test (BIST) circuit to accommodate in-circuit testing and diagnostics. The BIST circuit can be used to test the integrity of transmit and receive data paths. The BIST can be performed using both internal loopbacks (digital or analog) or external loopback using a cable fixture. The BIST simulates pseudo-random data transfer scenarios in format of real packets and Inter-Packet Gap (IPG) on the lines. The BIST allows full control of the packet lengths and the IPG.

7.4 Device Functional Modes

DP83TD510E can be used in MII Mode, RMII Master Mode and Slave Mode. Refer to RMII section for connection diagram.

7.4.1 Straps Configuration

The DP83TD510E uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset. During software resets, the strap options are internally reloaded from the values sampled at power up or hard reset. The strap option pin assignments are defined below. Configuration of the device may be done through the strap pins or through the management register interface. A pullup resistor or a pulldown resistor of suggested values may be used to set the voltage ratio of the strap pin input and the supply to select one of the possible selected modes. The MAC interface pins must support I/O voltages of 3.3 V, 2.5 V, and 1.8 V. As the strap inputs are implemented on these pins, the straps must also support operation at 3.3-V, 2.5-V, and 1.8-V supplies depending on what voltage was selected for I/O. All strap pins have two levels.

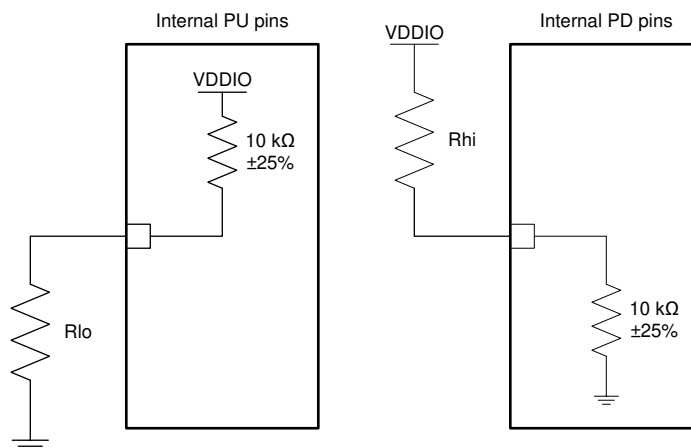


Figure 7-6. Strap Circuit

Table 7-4. 2-Level Strap Resistor Ratio

| MODE | IDEAL RESISTORS | |
|------|-----------------|----------|
| | Rhi (kΩ) | Rlo (kΩ) |
| 0 | OPEN | 2.49 |
| 1 | 2.49 | OPEN |

7.4.1.1 Straps for PHY Address

Table 7-5. PHY Address Strap Table

| PIN NAME | STRAP NAME | PIN # | DEFAULT | | |
|----------|------------|-------|---------|--------|----------|
| GPIO1 | Strap9 | 32 | 0 | | PHY_ADD0 |
| | | | | MODE 0 | 0 |
| | | | | MODE 1 | 1 |
| RX_ERR | Strap6 | 20 | 0 | | PHY_ADD1 |
| | | | | MODE 0 | 0 |
| | | | | MODE 1 | 1 |
| RX_D0 | Strap4 | 16 | 0 | | PHY_ADD2 |
| | | | | MODE 0 | 0 |
| | | | | MODE 1 | 1 |
| RX_D3 | Strap1 | 13 | 0 | | PHY_ADD3 |
| | | | | MODE 0 | 0 |
| | | | | MODE 1 | 1 |

PHY Address strap is 4 bit strap on pin 13, 16, 20 and 32. It shall be read as [3:2:1:0] respectively. Default PHY Address is 0000.

Table 7-6. Reach Selection Strap

| PIN NAME | STRAP NAME | PIN # | DEFAULT | | |
|----------|------------|-------|---------|---|---|
| LED_2 | Strap7 | 28 | 0 | 0 | This Strap defines the voltage level requested by PHY during auto negotiation. It is reflected in bit 12 of 0x20E. While using Force mode for Linkup, the strap controls the output voltage and reflects in bit 12 of 0x18F6 0 : 1-V p2p 1: 2.4-V p2p |
| | | | | 1 | |

Table 7-7. MAC Mode Strap Table

| PIN NAME | STRAP NAME | PIN # | DEFAULT | Strap8 | Strap3 | |
|----------|------------|-------|---------|--------|--------|---------------|
| RX_D1 | Strap3 | 15 | 0 | 0 | 0 | MII (default) |
| | | | | 0 | 1 | RMII Master |
| LED_0 | Strap8 | 29 | 0 | 1 | 0 | Reserved |
| | | | | 1 | 1 | RMII Slave |

Table 7-8. RMII MAC Mode Strap Table

| PIN NAME | STRAP NAME | PIN # | DEFAULT | | |
|----------|------------|-------|---------|---|---|
| RX_D2 | Strap2 | 14 | 0 | 0 | CRS_DV/RX_DV Pin 18 is configured as CRS_DV (default) |
| | | | | 1 | CRS_DV/RX_DV Pin 18 is configured as RX_DV (For RMII Repeater Mode) |

Table 7-9. Terminations Selection

| PIN NAME | STRAP NAME | PIN # | DEFAULT | | |
|----------|------------|-------|-----------------|---|---|
| GPIO2 | Strap10 | 8 | Mandatory PU/PD | 0 | Receiver with tapping at 50 Ω (Recommended) |
| | | | | 1 | Receiver tapping at < 40 Ω |

Table 7-10. Clockout/LED_1

| PIN NAME | STRAP NAME | PIN # | DEFAULT | | |
|--------------|------------|-------|---------|---|-------------------------|
| RX_DV/CRS_DV | Strap5 | 18 | 0 | 0 | Clockout 25 M(default) |
| | | | | 1 | LED1 |

7.5 Programming

DP83TD510E provides an IEEE defined register set for programming and status. It also provides an additional register set to configure other features not supported thru IEEE registers.

7.6 MMD Register Address Map

Table 7-11. MMD Register Map Address Table

| Register Address Range | MMD | Example Usage |
|---------------------------------|------|--------------------------|
| 0x1000 to 0x18F8 | 0x1 | MMD=0x1, Address=0x08F8 |
| 0x3000 to 0x38E7 | 0x3 | MMD=0x3, Address=0x08E7 |
| 0x200 to 0x20F | 0x7 | MMD=07, Address=0x20F |
| 0x0000 to 0x0130, 0x0300-0x0E01 | 0x1F | MMD=0x1F, Address=0x0000 |

7.7 DP83TD510E Registers

Table 7-12 lists the DP83TD510E registers. All register offset addresses not listed in Table 7-12 should be considered as reserved locations and the register contents should not be modified.

DP83TD51010BaseT1L

Table 7-12. DP83TD510E Registers

| Address | Acronym | Register Name | Section |
|---------|-----------------|---------------|--------------------|
| 0x0 | MII_REG_0 | | Go |
| 0x10 | PHY_STS | | Go |
| 0x11 | GEN_CFG | | Go |
| 0x12 | INTERRUPT_REG_1 | | Go |
| 0x13 | INTERRUPT_REG_2 | | Go |
| 0x15 | RX_ERR_CNT | | Go |
| 0x16 | BISCR | | Go |
| 0x17 | MAC_CFG_1 | | Go |
| 0x18 | MAC_CFG_2 | | Go |
| 0x19 | SOR_PHYAD | | Go |
| 0x1E | TDR_CFG | | Go |
| 0x119 | PRBS_CFG_1 | | Go |
| 0x11A | PRBS_CFG_2 | | Go |
| 0x11B | PRBS_CFG_3 | | Go |
| 0x11C | PRBS_STATUS_1 | | Go |
| 0x11D | PRBS_STATUS_2 | | Go |
| 0x11E | PRBS_STATUS_3 | | Go |
| 0x11F | PRBS_STATUS_4 | | Go |
| 0x120 | PRBS_STATUS_5 | | Go |
| 0x121 | PRBS_STATUS_6 | | Go |
| 0x122 | PRBS_STATUS_7 | | Go |
| 0x123 | PRBS_CFG_4 | | Go |
| 0x124 | PRBS_CFG_5 | | Go |
| 0x125 | PRBS_CFG_6 | | Go |
| 0x126 | PRBS_CFG_7 | | Go |
| 0x127 | PRBS_CFG_8 | | Go |
| 0x128 | PRBS_CFG_9 | | Go |
| 0x129 | PRBS_CFG_10 | | Go |
| 0x12A | CRC_STATUS | | Go |
| 0x12B | PKT_STAT_1 | | Go |
| 0x12C | PKT_STAT_2 | | Go |
| 0x12D | PKT_STAT_3 | | Go |
| 0x12E | PKT_STAT_4 | | Go |
| 0x12F | PKT_STAT_5 | | Go |
| 0x130 | PKT_STAT_6 | | Go |
| 0x200 | AN_CONTROL | | Go |
| 0x201 | AN_STATUS | | Go |
| 0x202 | AN_ADV_1 | | Go |
| 0x203 | AN_ADV_2 | | Go |
| 0x204 | AN_ADV_3 | | Go |

Table 7-12. DP83TD510E Registers (continued)

| Address | Acronym | Register Name | Section |
|---------|----------------------------|---------------|--------------------|
| 0x205 | AN_LP_ADV_1 | | Go |
| 0x206 | AN_LP_ADV_2 | | Go |
| 0x207 | AN_LP_ADV_3 | | Go |
| 0x208 | AN_NP_ADV_1 | | Go |
| 0x209 | AN_NP_ADV_2 | | Go |
| 0x20A | AN_NP_ADV_3 | | Go |
| 0x20B | AN_LP_NP_ADV_1 | | Go |
| 0x20C | AN_LP_NP_ADV_2 | | Go |
| 0x20D | AN_LP_NP_ADV_3 | | Go |
| 0x20E | AN_CTRL_10BT1 | | Go |
| 0x20F | AN_STATUS_10BT1 | | Go |
| 0x460 | LEDS_CFG_1 | | Go |
| 0x461 | IO_MUX_CFG | | Go |
| 0x462 | IO_MUX_GPIO_CTRL_1 | | Go |
| 0x463 | IO_MUX_GPIO_CTRL_2 | | Go |
| 0x467 | CHIP_SOR_1 | | Go |
| 0x468 | CHIP_SOR_2 | | Go |
| 0x469 | LEDS_CFG_2 | | Go |
| 0x60C | AN_STAT_1 | | Go |
| 0x872 | dsp_reg_72 | | Go |
| 0xE01 | SCAN_2 | | Go |
| 0x1000 | PAM_PMD_CTRL_1 | | Go |
| 0x1007 | PMA_PMD_CTRL_2 | | Go |
| 0x100B | PMA_PMD_EXTENDED_ABILITY_2 | | Go |
| 0x1012 | PMA_PMD_EXTENDED_ABILITY | | Go |
| 0x1834 | PMA_PMD_CTRL | | Go |
| 0x18F6 | PMA_CTRL | | Go |
| 0x18F7 | PMA_STATUS | | Go |
| 0x18F8 | TEST_MODE_CTRL | | Go |
| 0x3000 | PCS_CTRL | | Go |
| 0x38E6 | PCS_CTRL_2 | | Go |
| 0x38E7 | PCS_STATUS | | Go |

Complex bit access types are encoded to fit into small table cells. [Table 7-13](#) shows the codes that are used for access types in this section.

Table 7-13. DP83TD510E Access Type Codes

| Access Type | Code | Description |
|-------------|---------|---------------------|
| Read Type | | |
| R | R | Read |
| Write Type | | |
| W | W | Write |
| W0C | W 0C | Write 0 to clear |
| W0S | W 0S | Write 0 to set |

Table 7-13. DP83TD510E Access Type Codes (continued)

| Access Type | Code | Description |
|------------------------|------|--|
| WMC | W | Write |
| WSC | W | Write |
| Reset or Default Value | | |
| - n | | Value after reset or the default value |

7.7.1 MII_REG_0 Register (Address = 0x0) [reset = 0x0]

MI_REG_0 is shown in [Table 7-14](#).

Return to the [Summary Table](#).

Table 7-14. MII_REG_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------|-------|-------|--|
| 15 | mii_reset | R/WSC | 0x0 | 1b = Digital in reset and all MII regs (0x0 - 0xF) as well as interrupt status are reset to default 0b = No reset |
| 14 | loopback | R/WMC | 0x0 | 1b = MII loopback 0b = No MII loopback |
| 13 | RESERVED | R | 0x0 | Reserved |
| 12 | RESERVED | R | 0x0 | Reserved |
| 11 | power_down | R/WMC | 0x0 | 1b = Power down via register or pin 0b = Normal mode |
| 10 | isolate | R/WMC | 0x0 | 1b = Isolate mode 0b = Normal mode |
| 9 | RESERVED | R | 0x0 | Reserved |
| 8 | RESERVED | R | 0x0 | Reserved |
| 7 | RESERVED | R | 0x0 | Reserved |
| 6 | RESERVED | R | 0x0 | Reserved |
| 5 | unidirectional_ability | R | 0x0 | Reserved |
| 4-0 | RESERVED | R | 0x0 | |

7.7.2 PHY_STS Register (Address = 0x10) [reset = 0x0]

PHY_STS is shown in [Table 7-15](#).

Return to the [Summary Table](#).

Table 7-15. PHY_STS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|-------|-------|--|
| 15-8 | RESERVED | R | 0x0 | |
| 7 | mii_interrupt | R/WOC | 0x0 | 1b = Interrupt pin had been set 0b = Interrupts pin not set |
| 6-1 | RESERVED | R | 0x0 | |
| 0 | link_status | R | 0x0 | 1b = Link is up 0b = Link is down |

7.7.3 GEN_CFG Register (Address = 0x11) [reset = 0x2A]

GEN_CFG is shown in [Table 7-16](#).

Return to the [Summary Table](#).

Table 7-16. GEN_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 15 | dis_clk_125 | R/W | 0x0 | 1b = Disable CLK_125 0b = Enable CLK_125 |
| 14 | pwr_save_mode_en | R/W | 0x0 | Enable power save mode |
| 13-12 | pwr_save_mode | R/W | 0x0 | 00b = Normal mode 01b = IEEE mode 1xb = Reserved |
| 11 | channel_debug_mode | R/W | 0x0 | |
| 10 | debug_mode | R/W | 0x0 | To reduce simulation time |
| 9-7 | RESERVED | R | 0x0 | |
| 6-5 | tx_fifo_depth | R/W | 0x1 | Fifo depth for RMII Tx fifo 00b = 4 nibbles 01b = 5 nibbles 10b = 6 nibbles 11b = 8 nibbles |
| 4 | RESERVED | R | 0x0 | |
| 3 | int_polarity | R/W | 0x1 | 1b = Interrupt pin is active low 0b = Interrupt pin active high |
| 2 | force_interrupt | R/W | 0x0 | Force interrupt pin to be active |
| 1 | int_en | R/W | 0x1 | 1b = Enable interrupt 0b = Disable interrupt |
| 0 | int_oe | R/W | 0x0 | 1b = MDINT_PWDN is interrupt pin 0b = MDINT_PWDN is power down pin |

7.7.4 INTERRUPT_REG_1 Register (Address = 0x12) [reset = 0x0]

INTERRUPT_REG_1 is shown in [Table 7-17](#).

Return to the [Summary Table](#).

Table 7-17. INTERRUPT_REG_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|---|
| 15 | rhf_int | R | 0x0 | Rx error cnt half full int status Note : Latch high until read |
| 14 | RESERVED | R | 0x0 | |
| 13 | link_int | R | 0x0 | Link status change interrupt status Note : Latch high until clear |
| 12 | RESERVED | R | 0x0 | Reserved |
| 11 | esd_int | R | 0x0 | ESD interrupt status Note : Latch high until clear |
| 10-8 | RESERVED | R | 0x0 | |
| 7 | rhf_int_en | R/W | 0x0 | 1b = Enable rx_err_cnt half full interrupt 0b = Disable rx_err_cnt half full interrupt |
| 6 | RESERVED | R | 0x0 | |
| 5 | link_int_en | R/W | 0x0 | 1b = Enable link status change interrupt 0b = Disable link status change interrupt |
| 4 | RESERVED | R | 0x0 | Reserved |
| 3 | esd_int_en | R/W | 0x0 | 1b = Enable ESD interrupt 0b = Dsiable ESD interrupt |
| 2-0 | RESERVED | R | 0x0 | |

7.7.5 INTERRUPT_REG_2 Register (Address = 0x13) [reset = 0x0]

INTERRUPT_REG_2 is shown in [Table 7-18](#).

Return to the [Summary Table](#).

Table 7-18. INTERRUPT_REG_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 15-14 | RESERVED | R | 0x0 | |
| 13 | page_int | R | 0x0 | Aneg page received interrupt status Note : Latch high until clear |
| 12-10 | RESERVED | R | 0x0 | |
| 9 | pol_int | R | 0x0 | Polarity change interrupt status Note : Latch high until clear |
| 8 | por_done_int | R | 0x0 | POR done interrupt status Note : Latch high until clear |
| 7-6 | RESERVED | R | 0x0 | |
| 5 | page_int_en | R/W | 0x0 | 1b = Enable aneg page received interrupt 0b = Disable aneg page received interrupt |
| 4-2 | RESERVED | R | 0x0 | |
| 1 | pol_int_en | R/W | 0x0 | 1b = Enable polarity change interrupt 0b = Disable polarity change interrupt |
| 0 | por_done_int_en | R/W | 0x0 | 1b = Enable POR done interrupt 0b = Disable POR done interrupt |

7.7.6 RX_ERR_CNT Register (Address = 0x15) [reset = 0x0]

RX_ERR_CNT is shown in [Table 7-19](#).

Return to the [Summary Table](#).

Table 7-19. RX_ERR_CNT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 15-0 | rx_err_cnt | R | 0x0 | Counts number of RX_ERR, saturates on max value Note : Clear on read |

7.7.7 BISCRC Register (Address = 0x16) [reset = 0x100]

BISCRC is shown in [Table 7-20](#).

Return to the [Summary Table](#).

Table 7-20. BISCRC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 15-9 | RESERVED | R | 0x0 | |
| 8 | core_pwr_mode | R | 0x1 | 1b = Core is in normal power mode 0b = Core is in power down/sleep mode |
| 7 | RESERVED | R | 0x0 | |
| 6-0 | loopback_mode | R/W | 0x0 | 0000001b = Reserved 0000010b = PCS loopback (Tx PAM3 to Rx PAM3) 0000100b = Digital loopback 0001000b = Analog loopback 0010000b = Reverse loopback 0100000b = Transmit to MAC in reverse loopback 1000000b = Transmit to MDI in MAC loopback |

7.7.8 MAC_CFG_1 Register (Address = 0x17) [reset = 0x4001]

MAC_CFG_1 is shown in [Table 7-21](#).

Return to the [Summary Table](#).

Table 7-21. MAC_CFG_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|-------|-------|--|
| 15 | cfg_rmii_dis_delayed_txd_en | R/W | 0x0 | Reserved |
| 14 | min_ipg_mode_en | R/W | 0x1 | |
| 13 | cfg_rmii_enh | R/W | 0x0 | |
| 12 | cfg_rgmii_rx_clk_shift_sel | R/W | 0x0 | 1b = RGMII RX clock and data are shifted 0b = RGMII RX clock and data are aligned |
| 11 | cfg_rgmii_tx_clk_shift_sel | R/W | 0x0 | 0b = RGMII TX clock and data are shifted 1b = RGMII TX clock and data are aligned |
| 10 | RESERVED | R | 0x0 | |
| 9 | cfg_rgmii_en | R/W | 0x0 | 1b = RGMII enable 0b = RGMII disable |
| 8 | cfg_rmii_clk_shift_en | R/W | 0x0 | Reserved |
| 7 | cfg_xi_50 | R/W | 0x0 | 1b = XI is 50MHz 0b = XI is 25MHz |
| 6 | cfg_rmii_slow_mode | R/W | 0x0 | In RMII recovered clock mode, bypass async fifo |
| 5 | cfg_rmii_mode | R/W | 0x0 | 1b = RMII MAC 0b = MII MAC (0x17[9] should be disabled) |
| 4 | cfg_rmii_rev1_0 | R/W | 0x0 | 1b = RMII rev1.0 (CRS_DV will toggle at the end of a packet to indicate deassertion of CRS) 0b = RMII rev1.2 (CRS_DV will remain asserted until final data is transferred. CRS_DV will not toggle at the end of a packet) |
| 3 | rmii_ovf_sts | R/W0C | 0x0 | RMII fifo overflow indication |
| 2 | rmii_unf_sts | R/W0C | 0x0 | RMII fifo underflow indication |
| 1-0 | cfg_rmii_elast_buf | R/W | 0x1 | RMII rx fifo 00b = 14 bit tolerance (upto 16800 byte packet) 01b = 2 bit tolerance (upto 2400 byte packet) 10b = 6 bit tolerance (upto 7200 byte packet) 11b = 10 bit tolerance (upto 12000 byte packet) |

7.7.9 MAC_CFG_2 Register (Address = 0x18) [reset = 0x3]

MAC_CFG_2 is shown in [Table 7-22](#).

Return to the [Summary Table](#).

Table 7-22. MAC_CFG_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 15-12 | RESERVED | R | 0x0 | |
| 11 | cfg_inv_rx_clk | R/W | 0x0 | |
| 10 | cfg_rmii_crs_dv_sel | R/W | 0x0 | 1b = CRS is sent out on RX_CTRL for RMII 0b = DV is sent out on RX_CTRL for RMII |
| 9 | rgmii_tx_af_empty_err | R | 0x0 | |
| 8 | rgmii_tx_af_full_err | R | 0x0 | |
| 7-6 | RESERVED | R | 0x0 | Reserved |

Table 7-22. MAC_CFG_2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------|------|-------|--|
| 5 | inv_rgmii_rxd | R/W | 0x0 | Swap 3:0 to 0:3 |
| 4 | inv_rgmii_txd | R/W | 0x0 | Swap 3:0 to 0:3 |
| 3 | sup_tx_err_fd_rgmii | R/W | 0x0 | 1b = Suppress tx_err in full duplex when tx_en not active (CEXT) 0b = Normal |
| 2-0 | cfg_rgmii_half_full_th | R/W | 0x3 | RGMII TX sync FIFO half full threshold. Option to reduce latency for RGMII: If the MAC and PHY are fed by same clock source (no PPM) we can lower the threshold from 2 to 1. |

7.7.10 SOR_PHYAD Register (Address = 0x19) [reset = 0x0]

SOR_PHYAD is shown in [Table 7-23](#).

Return to the [Summary Table](#).

Table 7-23. SOR_PHYAD Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|-------------|
| 15-5 | RESERVED | R | 0x0 | |
| 4-0 | SOR_PHYADDR | R | 0x0 | |

7.7.11 TDR_CFG Register (Address = 0x1E) [reset = 0x0]

TDR_CFG is shown in [Table 7-24](#).

Return to the [Summary Table](#).

Table 7-24. TDR_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|--------|-------|---|
| 15 | tdr_start | R/W/MC | 0x0 | Start TDR procedure |
| 14 | cfg_tdr_auto_run | R/W | 0x0 | 1b = Enable TDR auto start on link down 0b = TDR should be manually enabled by configuration |
| 13-2 | RESERVED | R | 0x0 | |
| 1 | tdr_done | R | 0x0 | TDR done indication (only valid once TDR is started) |
| 0 | tdr_fail | R | 0x0 | TDR fail indication |

7.7.12 PRBS_CFG_1 Register (Address = 0x119) [reset = 0x574]

PRBS_CFG_1 is shown in [Table 7-25](#).

Return to the [Summary Table](#).

Table 7-25. PRBS_CFG_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|--------|-------|---|
| 15-13 | RESERVED | R | 0x0 | |
| 12 | send_pkt | R/W/MC | 0x0 | Enables generating MAC packet with fix/incremental data w CRC (pkt_gen_en has to be set and cfg_pkt_gen_prbs has to be clear) Cleared automatically when pkt_done is set |
| 11 | RESERVED | R | 0x0 | |

Table 7-25. PRBS_CFG_1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|--|
| 10-8 | cfg_prbs_chk_sel | R/W | 0x5 | 000 : Checker receives from RGMII TX 010 : Checker receives from RMII TX 011 : Checker receives from MII TX 101 : Checker receives from Cu RX |
| 7 | RESERVED | R | 0x0 | |
| 6-4 | cfg_prbs_gen_sel | R/W | 0x7 | 000 : PRBS transmits to RGMII RX 010 : PRBS transmits to RMII RX 011 : PRBS transmits to MII RX 101 : PRBS transmits to Cu TX |
| 3 | cfg_prbs_cnt_mode | R/W | 0x0 | 1 = Continuous mode, when one of the PRBS counters reaches max value, pulse is generated and counter starts counting from zero again 0 = Single mode, When one of the PRBS counters reaches max value, PRBS checker stops counting. |
| 2 | cfg_prbs_chk_enable | R/W | 0x1 | Enable PRBS checker xbar (to receive data) To be enabled for rx packet counters to work |
| 1 | cfg_pkt_gen_prbs | R/W | 0x0 | If set: (1) When pkt_gen_en is set, PRBS packets are generated continuously (3) When pkt_gen_en is cleared, PRBS RX checker is still enabled If cleared: (1) When pkt_gen_en is set, non - PRBS packet is generated (3) When pkt_gen_en is cleared, PRBS RX checker is disabled as well |
| 0 | pkt_gen_en | R/W | 0x0 | 1 = Enable packet/PRBS generator 0 = Disable packet/PRBS generato |

7.7.13 PRBS_CFG_2 Register (Address = 0x11A) [reset = 0x5DC]

PRBS_CFG_2 is shown in [Table 7-26](#).

Return to the [Summary Table](#).

Table 7-26. PRBS_CFG_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 15-0 | cfg_pkt_len_prbs | R/W | 0x5DC | Length (in bytes) of PRBS packets and MAC packets w CRC |

7.7.14 PRBS_CFG_3 Register (Address = 0x11B) [reset = 0x7D]

PRBS_CFG_3 is shown in [Table 7-27](#).

Return to the [Summary Table](#).

Table 7-27. PRBS_CFG_3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---|
| 15-13 | RESERVED | R | 0x0 | |
| 12 | cfg_prbs_fix_patt_en | R/W | 0x0 | |
| 11-8 | cfg_prbs_fix_patt | R/W | 0x0 | |
| 7-0 | cfg_ipg_len | R/W | 0x7D | Inter-packet gap (in bytes) between packets |

7.7.15 PRBS_STATUS_1 Register (Address = 0x11C) [reset = 0x0]

PRBS_STATUS_1 is shown in [Table 7-28](#).

Return to the [Summary Table](#).

Table 7-28. PRBS_STATUS_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 15-0 | prbs_byte_cnt | R | 0x0 | Holds number of total bytes that received by the PRBS checker. Value in this register is locked when write is done to register 0x11F bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFF |

7.7.16 PRBS_STATUS_2 Register (Address = 0x11D) [reset = 0x0]

 PRBS_STATUS_2 is shown in [Table 7-29](#).

 Return to the [Summary Table](#).

Table 7-29. PRBS_STATUS_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|---|
| 15-0 | prbs_pkt_cnt_15_0 | R | 0x0 | Bits [15:0] of number of total packets received by the PRBS checker Value in this register is locked when write is done to register 0x11F bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF |

7.7.17 PRBS_STATUS_3 Register (Address = 0x11E) [reset = 0x0]

 PRBS_STATUS_3 is shown in [Table 7-30](#).

 Return to the [Summary Table](#).

Table 7-30. PRBS_STATUS_3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|--|
| 15-0 | prbs_pkt_cnt_31_16 | R | 0x0 | Bits [31:16] of number of total packets received by the PRBS checker Value in this register is locked when write is done to register 0x11F bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF |

7.7.18 PRBS_STATUS_4 Register (Address = 0x11F) [reset = 0x0]

 PRBS_STATUS_4 is shown in [Table 7-31](#).

 Return to the [Summary Table](#).

Table 7-31. PRBS_STATUS_4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|-------|-------|---|
| 15-14 | RESERVED | R | 0x0 | |
| 13 | prbs_sync_loss | R/W0C | 0x0 | 1b = PRBS has locked 0b = PRBS did not unlock |
| 12 | pkt_done | R | 0x0 | Set when all MAC packets w CRC are transmitted |
| 11 | pkt_gen_busy | R | 0x0 | 1 = Packet generator is in process 0 = Packet generator is not in process |
| 10 | prbs_pkt_ov | R | 0x0 | If set, packet counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit #1 of 0x11f |
| 9 | prbs_byte_ov | R | 0x0 | If set, bytes counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit #1 of 0x11f |
| 8 | prbs_lock | R | 0x0 | 1 = PRBS checker is locked sync) on received byte stream 0 = PRBS checker is not locked |

Table 7-31. PRBS_STATUS_4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7-0 | prbs_err_cnt | R | 0x0 | Holds number of errored bits received by the PRBS checker Value in this register is locked when write is done to bit[0] or bit[1] When PRBS Count Mode set to zero, count stops on 0xFF Notes: Writing bit 0 generates a lock signal for the PRBS counters. Writing bit 1 generates a lock and clear signal for the PRBS counters |

7.7.19 PRBS_STATUS_5 Register (Address = 0x120) [reset = 0x0]

PRBS_STATUS_5 is shown in [Table 7-32](#).

Return to the [Summary Table](#).

Table 7-32. PRBS_STATUS_5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|--|
| 15-8 | RESERVED | R | 0x0 | |
| 7-0 | prbs_err_ov_cnt | R | 0x0 | Holds number of error counter overflow that received by the PRBS checker. Value in this register is locked when write is done to register 0x11f bit[0] or bit[1]. Counter stops on 0xFF. Note: when PRBS counters work in single mode, overflow counter is not active |

7.7.20 PRBS_STATUS_6 Register (Address = 0x121) [reset = 0x0]

PRBS_STATUS_6 is shown in [Table 7-33](#).

Return to the [Summary Table](#).

Table 7-33. PRBS_STATUS_6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 15-0 | pkt_err_cnt_15_0 | R | 0x0 | Bits [15:0] of number of total packets with error received by the PRBS checker Value in this register is locked when write is done to register 0x11f bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF |

7.7.21 PRBS_STATUS_7 Register (Address = 0x122) [reset = 0x0]

PRBS_STATUS_7 is shown in [Table 7-34](#).

Return to the [Summary Table](#).

Table 7-34. PRBS_STATUS_7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|---|
| 15-0 | pkt_err_cnt_31_16 | R | 0x0 | Bits [31:16] of number of total packets with error received by the PRBS checker Value in this register is locked when write is done to register 0x11f bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF |

7.7.22 PRBS_CFG_4 Register (Address = 0x123) [reset = 0x0]

PRBS_CFG_4 is shown in [Table 7-35](#).

Return to the [Summary Table](#).

Table 7-35. PRBS_CFG_4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|---|
| 15-8 | cfg_pkt_data | R/W | 0x0 | Fixed data to be sent in Fix data mode |
| 7-6 | cfg_pkt_mode | R/W | 0x0 | 2'b 00 - Incremental 2'b 01 - Fixed 2'b1x - PRBS |
| 5-3 | cfg_pattern_vld_bytes | R/W | 0x0 | Number of bytes of valid pattern in packet (Max - 6) |
| 2-0 | cfg_pkt_cnt | R/W | 0x0 | 000b = 1 packet 001b = 10 packets 010b = 100 packets 011b = 1000 packets 100b = 10000 packets 101b = 100000 packets 110b = 1000000 packets 111b = Continuous packets |

7.7.23 PRBS_CFG_5 Register (Address = 0x124) [reset = 0x0]

 PRBS_CFG_5 is shown in [Table 7-36](#).

 Return to the [Summary Table](#).

Table 7-36. PRBS_CFG_5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|----------------------|
| 15-0 | pattern_15_0 | R/W | 0x0 | Bits 15:0 of pattern |

7.7.24 PRBS_CFG_6 Register (Address = 0x125) [reset = 0x0]

 PRBS_CFG_6 is shown in [Table 7-37](#).

 Return to the [Summary Table](#).

Table 7-37. PRBS_CFG_6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-----------------------|
| 15-0 | pattern_31_16 | R/W | 0x0 | Bits 31:16 of pattern |

7.7.25 PRBS_CFG_7 Register (Address = 0x126) [reset = 0x0]

 PRBS_CFG_7 is shown in [Table 7-38](#).

 Return to the [Summary Table](#).

Table 7-38. PRBS_CFG_7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-----------------------|
| 15-0 | pattern_47_32 | R/W | 0x0 | Bits 47:32 of pattern |

7.7.26 PRBS_CFG_8 Register (Address = 0x127) [reset = 0x0]

 PRBS_CFG_8 is shown in [Table 7-39](#).

 Return to the [Summary Table](#).

Table 7-39. PRBS_CFG_8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 15-0 | pmatch_data_15_0 | R/W | 0x0 | Bits 15:0 of Perfect Match Data - used for DA (destination address) match |

7.7.27 PRBS_CFG_9 Register (Address = 0x128) [reset = 0x0]

PRBS_CFG_9 is shown in [Table 7-40](#).

Return to the [Summary Table](#).

Table 7-40. PRBS_CFG_9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 15-0 | pmatch_data_31_16 | R/W | 0x0 | Bits 31:16 of Perfect Match Data - used for DA (destination address) match |

7.7.28 PRBS_CFG_10 Register (Address = 0x129) [reset = 0x0]

PRBS_CFG_10 is shown in [Table 7-41](#).

Return to the [Summary Table](#).

Table 7-41. PRBS_CFG_10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 15-0 | pmatch_data_47_32 | R/W | 0x0 | Bits 47:32 of Perfect Match Data - used for DA (destination address) match |

7.7.29 CRC_STATUS Register (Address = 0x12A) [reset = 0x0]

CRC_STATUS is shown in [Table 7-42](#).

Return to the [Summary Table](#).

Table 7-42. CRC_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 15-2 | RESERVED | R | 0x0 | |
| 1 | rx_bad_crc | R | 0x0 | CRC error indication in packet received on Cu RX |
| 0 | tx_bad_crc | R | 0x0 | CRC error indication in packet transmitted on Cu TX |

7.7.30 PKT_STAT_1 Register (Address = 0x12B) [reset = 0x0]

PKT_STAT_1 is shown in [Table 7-43](#).

Return to the [Summary Table](#).

Table 7-43. PKT_STAT_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|--|
| 15-0 | tx_pkt_cnt_15_0 | | 0x0 | Lower 16 bits of Tx packet counter Note : Register is cleared when 0x12B, 0x12C, 0x12D are read in sequence |

7.7.31 PKT_STAT_2 Register (Address = 0x12C) [reset = 0x0]

PKT_STAT_2 is shown in [Table 7-44](#).

Return to the [Summary Table](#).

Table 7-44. PKT_STAT_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 15-0 | tx_pkt_cnt_31_16 | | 0x0 | Upper 16 bits of Tx packet counter Note : Register is cleared when 0x12B, 0x12C, 0x12D are read in sequence |

7.7.32 PKT_STAT_3 Register (Address = 0x12D) [reset = 0x0]

PKT_STAT_3 is shown in [Table 7-45](#).

Return to the [Summary Table](#).

Table 7-45. PKT_STAT_3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|---|
| 15-0 | tx_err_pkt_cnt | | 0x0 | Tx packet w error (CRC error) counter Note : Register is cleared when 0x12B, 0x12C, 0x12D are read in sequence |

7.7.33 PKT_STAT_4 Register (Address = 0x12E) [reset = 0x0]

PKT_STAT_4 is shown in [Table 7-46](#).

Return to the [Summary Table](#).

Table 7-46. PKT_STAT_4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|--|
| 15-0 | rx_pkt_cnt_15_0 | | 0x0 | Lower 16 bits of Rx packet counter Note : Register is cleared when 0x12E, 0x12F, 0x130 are read in sequence |

7.7.34 PKT_STAT_5 Register (Address = 0x12F) [reset = 0x0]

PKT_STAT_5 is shown in [Table 7-47](#).

Return to the [Summary Table](#).

Table 7-47. PKT_STAT_5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 15-0 | rx_pkt_cnt_31_16 | | 0x0 | Upper 16 bits of Rx packet counter Note : Register is cleared when 0x12E, 0x12F, 0x130 are read in sequence |

7.7.35 PKT_STAT_6 Register (Address = 0x130) [reset = 0x0]

PKT_STAT_6 is shown in [Table 7-48](#).

Return to the [Summary Table](#).

Table 7-48. PKT_STAT_6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|---|
| 15-0 | rx_err_pkt_cnt | | 0x0 | Rx packet w error (CRC error) counter Note : Register is cleared when 0x12E, 0x12F, 0x130 are read in sequence |

7.7.36 AN_CONTROL Register (Address = 0x200) [reset = 0x1000]

AN_CONTROL is shown in [Table 7-49](#).

Return to the [Summary Table](#).

Table 7-49. AN_CONTROL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|-------|-------|---|
| 15 | mr_main_reset | R | 0x0 | 1 = AN reset 0 = AN normal operation Note : Bit is self clearing |
| 14-13 | RESERVED | R | 0x0 | |
| 12 | mr_an_enable | R/W | 0x1 | 1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process |
| 11-10 | RESERVED | R | 0x0 | |
| 9 | mr_restart_an | R/WSC | 0x0 | 1 = Restart Auto-Negotiation process 0 = Auto-Negotiation in process, disabled, or not supported |
| 8-0 | RESERVED | R | 0x0 | |

7.7.37 AN_STATUS Register (Address = 0x201) [reset = 0x8]

AN_STATUS is shown in [Table 7-50](#).

Return to the [Summary Table](#).

Table 7-50. AN_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|-------|-------|--|
| 15-7 | RESERVED | R | 0x0 | |
| 6 | mr_page_received | R/W0C | 0x0 | 1 = A page has been received 0 = A page has not been received |
| 5 | mr_an_complete | R | 0x0 | 1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed |
| 4 | remote_fault | R/W0C | 0x0 | 1 = remote fault condition detected 0 = no remote fault condition detected |
| 3 | mr_an_ability | R | 0x1 | 1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation |
| 2 | link_status | R/W0S | 0x0 | 1 = Link is up 0 = Link is down |
| 1-0 | RESERVED | R | 0x0 | |

7.7.38 AN_ADV_1 Register (Address = 0x202) [reset = 0x1]

AN_ADV_1 is shown in [Table 7-51](#).

Return to the [Summary Table](#).

Table 7-51. AN_ADV_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|-------------|
| 15 | mr_bp_np_ability | R/W | 0x0 | |
| 14 | mr_bp_ack | R | 0x0 | Always 0 |
| 13 | mr_bp_remote_fault | R/W | 0x0 | |

Table 7-51. AN_ADV_1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|---|
| 12-5 | mr_bp_12_5 | R/W | 0x0 | Bit 12 - Force Master/Slave Bit 11: 10 - Pause Bit 9: 5 - Echoes nonce |
| 4-0 | selector_field | R/W | 0x1 | 00001b = IEEE802.3 |

7.7.39 AN_ADV_2 Register (Address = 0x203) [reset = 0x0]

 AN_ADV_2 is shown in [Table 7-52](#).

 Return to the [Summary Table](#).

Table 7-52. AN_ADV_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 15-0 | mr_bp_31_16 | R/W | 0x0 | Bit 20:16 - Transmitted nonce Bit 31:21 - A10 to A0 |

7.7.40 AN_ADV_3 Register (Address = 0x204) [reset = 0x0]

 AN_ADV_3 is shown in [Table 7-53](#).

 Return to the [Summary Table](#).

Table 7-53. AN_ADV_3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|-------------|
| 15-0 | mr_bp_47_32 | R/W | 0x0 | A26 to A11 |

7.7.41 AN_LP_ADV_1 Register (Address = 0x205) [reset = 0x0]

 AN_LP_ADV_1 is shown in [Table 7-54](#).

 Return to the [Summary Table](#).

Table 7-54. AN_LP_ADV_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|--------------------|
| 15-0 | mr_lp_bp_15_0 | R | 0x0 | LP' base page 15:0 |

7.7.42 AN_LP_ADV_2 Register (Address = 0x206) [reset = 0x0]

 AN_LP_ADV_2 is shown in [Table 7-55](#).

 Return to the [Summary Table](#).

Table 7-55. AN_LP_ADV_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|----------------------|
| 15-0 | mr_lp_bp_31_16 | R | 0x0 | LP's base page 31:16 |

7.7.43 AN_LP_ADV_3 Register (Address = 0x207) [reset = 0x0]

 AN_LP_ADV_3 is shown in [Table 7-56](#).

Return to the [Summary Table](#).

Table 7-56. AN_LP_ADV_3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|----------------------|
| 15-0 | mr_lp_bp_47_32 | R | 0x0 | LP's base page 47:32 |

7.7.44 AN_NP_ADV_1 Register (Address = 0x208) [reset = 0x0]

AN_NP_ADV_1 is shown in [Table 7-57](#).

Return to the [Summary Table](#).

Table 7-57. AN_NP_ADV_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------------|------|-------|--------------------------|
| 15 | mr_np_np_ability | R/W | 0x0 | |
| 14 | RESERVED | R | 0x0 | |
| 13 | mr_np_message_page | R/W | 0x0 | |
| 12 | mr_np_ack2 | R/W | 0x0 | |
| 11 | mr_np_toggle | R | 0x0 | |
| 10-0 | mr_np_msg_uniform_code_field | R/W | 0x0 | Predefined message codes |

7.7.45 AN_NP_ADV_2 Register (Address = 0x209) [reset = 0x0]

AN_NP_ADV_2 is shown in [Table 7-58](#).

Return to the [Summary Table](#).

Table 7-58. AN_NP_ADV_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|-------------|
| 15-0 | mr_np_uniform_code_field_1 | R/W | 0x0 | |

7.7.46 AN_NP_ADV_3 Register (Address = 0x20A) [reset = 0x0]

AN_NP_ADV_3 is shown in [Table 7-59](#).

Return to the [Summary Table](#).

Table 7-59. AN_NP_ADV_3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|-------------|
| 15-0 | mr_np_uniform_code_field_2 | R/W | 0x0 | |

7.7.47 AN_LP_NP_ADV_1 Register (Address = 0x20B) [reset = 0x0]

AN_LP_NP_ADV_1 is shown in [Table 7-60](#).

Return to the [Summary Table](#).

Table 7-60. AN_LP_NP_ADV_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|-------------|
| 15 | mr_lp_np_np_ability | R | 0x0 | |
| 14 | mr_lp_np_ack | R | 0x0 | |
| 13 | mr_lp_np_message_page | R | 0x0 | |

Table 7-60. AN_LP_NP_ADV_1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|---------------------------------|------|-------|--------------------------|
| 12 | mr_lp_np_ack2 | R | 0x0 | |
| 11 | mr_lp_np_toggle | R | 0x0 | |
| 10-0 | mr_lp_np_msg_uniform_code_field | R | 0x0 | Predefined message codes |

7.7.48 AN_LP_NP_ADV_2 Register (Address = 0x20C) [reset = 0x0]

AN_LP_NP_ADV_2 is shown in [Table 7-61](#).

Return to the [Summary Table](#).

Table 7-61. AN_LP_NP_ADV_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------------|------|-------|-------------|
| 15-0 | mr_lp_np_uniform_code_field_1 | R | 0x0 | |

7.7.49 AN_LP_NP_ADV_3 Register (Address = 0x20D) [reset = 0x0]

AN_LP_NP_ADV_3 is shown in [Table 7-62](#).

Return to the [Summary Table](#).

Table 7-62. AN_LP_NP_ADV_3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------------|------|-------|-------------|
| 15-0 | mr_lp_np_uniform_code_field_2 | R | 0x0 | |

7.7.50 AN_CTRL_10BT1 Register (Address = 0x20E) [reset = 0xA000]

AN_CTRL_10BT1 is shown in [Table 7-63](#).

Return to the [Summary Table](#).

Table 7-63. AN_CTRL_10BT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------------|------|-------|---|
| 15 | mr_10bt1_L_capability | R/W | 0x1 | 1 = Advertise PHY as 10BASE-T1L capable 0 = Do not advertise PHY as 10BASE-T1L capable |
| 14 | mr_ability_10bt1_L_eee | R/W | 0x0 | 1 = Advertise that the 10BASE-T1L PHY has EEE ability 0 = Do not advertise that the 10BASE-T1L PHY has EEE ability (default) |
| 13 | mr_ability_10bt1_L_incr_tx_rx_lvl | R/W | 0x1 | 1 = Advertise that the 10BASE-T1L PHY has increased transmit/receive level ability 0 = Do not advertise that the 10BASE-T1L PHY has increased transmit/receive level ability (default) |
| 12 | mr_10bt1_L_incr_tx_rx_lvl_rqst | R/W | 0x0 | 1 = Request 10BASE-T1L increased transmit level 0 = Do not request 10BASE-T1L increased transmit level (default) |
| 11-8 | RESERVED | R | 0x0 | |
| 7 | RESERVED | R | 0x0 | Reserved |
| 6 | RESERVED | R | 0x0 | Reserved |
| 5-0 | RESERVED | R | 0x0 | |

7.7.51 AN_STATUS_10BT1 Register (Address = 0x20F) [reset = 0x0]

AN_STATUS_10BT1 is shown in [Table 7-64](#).

Return to the [Summary Table](#).

Table 7-64. AN_STATUS_10BT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------------------|------|-------|--|
| 15 | mr_lp_10bt1_L_capability | R | 0x0 | 1 = Link partner is advertising PHY as 10BASE-T1L capable 0 = Link partner is not advertising PHY as 10BASE-T1L capable |
| 14 | mr_lp_ability_10bt1_L_eee | R | 0x0 | 1 = Link partner is advertising that the 10BASE-T1L PHY has EEE ability 0 = Link partner is not advertising that the 10BASE-T1L PHY has EEE ability |
| 13 | mr_lp_ability_10bt1_L_incr_tx_rx_lvl | R | 0x0 | 1 = Link partner is advertising that the 10BASE-T1L PHY has increased transmit/ receive level ability 0 = Link partner is not advertising that the 10BASE-T1L PHY has increased transmit/ receive level ability |
| 12 | mr_lp_10bt1_L_incr_tx_rx_lvl_rqst | R | 0x0 | 1 = Link partner is requesting 10BASE-T1L link partner increased transmit level 0 = Link partner is not requesting 10BASE-T1L link partner increased transmit level |
| 11-8 | RESERVED | R | 0x0 | |
| 7 | RESERVED | R | 0x0 | Reserved |
| 6 | RESERVED | R | 0x0 | Reserved |
| 5-0 | RESERVED | R | 0x0 | |

7.7.52 LEDS_CFG_1 Register (Address = 0x460) [reset = 0x548]

LEDS_CFG_1 is shown in [Table 7-65](#).

Return to the [Summary Table](#).

Table 7-65. LEDS_CFG_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 15 | RESERVED | R | 0x0 | Reserved |
| 14 | leds_bypass_stretching | R/W | 0x0 | 0 - Normal Operation 1 - Bypass LEDs stretching |
| 13-12 | leds_blink_rate | R/W | 0x0 | 00 = 20Hz (50mSec) 01 = 10Hz (100mSec) 10 = 5Hz (200mSec) 11 = 2Hz (500mSec) |
| 11-8 | led_2_option | R/W | 0x5 | Controls LED_2 sources (same as bits 3:0) |
| 7-4 | led_1_option | R/W | 0x4 | Controls LED_1 sources (same as bits 3:0) |

Table 7-65. LEDS_CFG_1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 3-0 | led_0_option | R/W | 0x8 | Controls LED_0 source: 0x 0 - link OK 0x 1 - TX/RX activity 0x 2 - TX activity 0x 3 - RX activity 0x 4 - LR 0x 5 - SR 0x 6 - LED SPEED : High for 10Base-T 0x 7 - Duplex mode 0x 8 - link + blink on activity w stretch option 0x 9 - blink on activity w stretch option 0xA - blink on tx activity w stretch option 0xB - blink on rx activity w stretch option 0xC - link_lost 0xD - PRBS error (toggles on error) 0xE - XMMI TX/RX Error with stretch option |

7.7.53 IO_MUX_CFG Register (Address = 0x461) [reset = 0x5]IO_MUX_CFG is shown in [Table 7-66](#).Return to the [Summary Table](#).**Table 7-66. IO_MUX_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 15 | io_oe_n_value | R/W | 0x0 | when io_oe_n_force_ctrl='1' the direction of all IOs except MDC, MDIO and RESET_N is controlled via this bit: 0 - output 1 - Input |
| 14 | io_oe_n_force_ctrl | R/W | 0x0 | Debug option - enables forcing the direction of all IOs, except MDC, MDIO and RESET_N. If set, IOs direction is controlled via bit #15 |
| 13-12 | pupd_value | R/W | 0x0 | when pupd_force_cntl='1' the value of the pull up/down is control via this register |
| 11 | pupd_force_cntl | R/W | 0x0 | when '1' : all the PADs pull up/down is forced via registers |
| 10-6 | RESERVED | R | 0x0 | Reserved |
| 5-4 | impedance_ctrl | R/W | 0x0 | MAC interface PAD impedance control bit #0 of this field is the slew control bit. If set to '1', slew rates will be faster (default is 0) |
| 3-2 | mac_rx_impedance_ctrl | R/W | 0x1 | MAC interface PAD impedance control bit #0 of this field is the slew control bit. If set to '1', slew rates will be faster (default is 0) |
| 1-0 | mac_tx_impedance_ctrl | R/W | 0x1 | MAC interface PAD impedance control bit #0 of this field is the slew control bit. If set to '1', slew rates will be faster (default is 0) |

7.7.54 IO_MUX_GPIO_CTRL_1 Register (Address = 0x462) [reset = 0x0]

IO_MUX_GPIO_CTRL_1 is shown in [Table 7-67](#).

Return to the [Summary Table](#).

Table 7-67. IO_MUX_GPIO_CTRL_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|--|
| 15 | led_2_clk_div_2_en | R/W | 0x0 | If led_2_gpio is configured to led_2_clk_source, Selects divide by 2 of clock at led_2_clk_source |
| 14-12 | led_2_clk_source | R/W | 0x0 | In case clk_out is MUXed to LED_2 IO, this field controls clk_out source: 0 - XI clock 1 - LD 30MHz clock (Free/recovered based Master/Slave) 2 - 30 MHz ADC clock (recovered) 3 - Free 60MHz clock 4 - 7.5MHz clock (Free/recovered based Master/Slave) 5 - 25MHz clock to PLL (XI or XI/2) 6 - 2.5MHz clock (Free/recovered based Master/Slave) |
| 11 | led_2_clk_inv_en | R/W | 0x0 | If led_2_gpio is configured to led_2_clk_source, Selects inversion of clock at led_2_clk_source |
| 10-8 | led_2_gpio_ctrl | R/W | 0x0 | controls the output of LED_2 IO: 0 - LED_2 1 - Clock out 2 - Interrupt 3 - 1'b0 4 - 1588 TX 5 - 1588 RX 6 - constant '0' 7 - constant '1' |
| 7 | led_0_clk_div_2_en | R/W | 0x0 | If led_0_gpio is configured to led_0_clk_source, Selects divide by 2 of clock at led_0_clk_source |
| 6-4 | led_0_clk_source | R/W | 0x0 | In case clk_out is MUXed to LED_0 IO, this field controls clk_out source: 0 - XI clock 1 - LD 30MHz clock (Free/recovered based Master/Slave) 2 - 30 MHz ADC clock (recovered) 3 - Free 60MHz clock 4 - 7.5MHz clock (Free/recovered based Master/Slave) 5 - 25MHz clock to PLL (XI or XI/2) 6 - 2.5MHz clock (Free/recovered based Master/Slave) |
| 3 | led_0_clk_inv_en | R/W | 0x0 | If led_0_gpio is configured to led_0_clk_source, Selects inversion of clock at led_0_clk_source |
| 2-0 | led_0_gpio_ctrl | R/W | 0x0 | controls the output of LED_0 IO: 0 - LED_0 1 - Clock out 2 - Interrupt 3 - 1'b0 4 - 1588 TX 5 - 1588 RX 6 - constant '0' 7 - constant '1' |

7.7.55 IO_MUX_GPIO_CTRL_2 Register (Address = 0x463) [reset = 0x0]

IO_MUX_GPIO_CTRL_2 is shown in [Table 7-68](#).

Return to the [Summary Table](#).

Table 7-68. IO_MUX_GPIO_CTRL_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 15-13 | gpio_clk_source | R/W | 0x0 | In case clk_out is MUXed to GPIO IO, this field controls clk_out source: 0 - XI clock 1 - LD 30MHz clock (Free/recovered based Master/Slave) 2 - 30 MHz ADC clock (recovered) 3 - Free 60MHz clock 4 - 7.5MHz clock (Free/recovered based Master/Slave) 5 - 25MHz clock to PLL (XI or XI/2) 6 - 2.5MHz clock (Free/recovered based Master/Slave) |
| 12-10 | gpio_ctrl | R/W | 0x0 | controls the output of GPIO IO: 0 - LED_1 1 - Clock out 2 - Interrupt 3 - 1'b0 4 - 1588 TX 5 - 1588 RX 6 - constant '0' 7 - constant '1' |
| 9 | cfg_tx_er_on_led2 | R/W | 0x0 | 1b = LED_2 is used as TX_ER pin for MII |
| 8 | clk_o_clk_div_2_en | R/W | 0x0 | If clk_out is configured to output clk_o_clk_source, Selects divide by 2 of clock at clk_o_clk_source |
| 7-4 | clk_o_clk_source | R/W | 0x0 | In case clk_out is MUXed to CLK_O IO, this field controls clk_out source: 0 - XI clock 1 - LD 30MHz clock (Free/recovered based Master/Slave) 2 - 30 MHz ADC clock (recovered) 3 - Free 60MHz clock 4 - 7.5MHz clock (Free/recovered based Master/Slave) 5 - 25MHz clock to PLL (XI or XI/2) 6 - 2.5MHz clock (Free/recovered based Master/Slave) 8 - CLK25_50 (50 MHz in RMII, 25 MHz in others) 9 - RMII RX 50MHz clock 10 - RMII TX 50MHz clock 11 - MII RX clock 12 - RGMII RX align clock 13 - RGMII RX shift clock |
| 3 | clk_o_clk_inv_en | R/W | 0x0 | If clk_out is configured to output clk_o_clk_source, Selects inversion of clock at clk_o_clk_source |
| 2-0 | clk_o_gpio_ctrl | R/W | 0x0 | controls the output of CLK_O IO: 0 - LED_1 1 - Clock out 2 - Interrupt 3 - 1'b0 4 - 1588 TX 5 - 1588 RX 6 - constant '0' 7 - constant '1' |

7.7.56 CHIP_SOR_1 Register (Address = 0x467) [reset = 0x0]CHIP_SOR_1 is shown in [Table 7-69](#).Return to the [Summary Table](#).

Table 7-69. CHIP_SOR_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 15-0 | sor_15_0 | R | 0x0 | SOR vector, bits [15:0] : SOR[0] - RX_D3 SOR[1] - RX_D2 SOR[2] - RX_D1 SOR[3] - RX_D0 SOR[5] - RX_CTRL SOR[6] - RX_ER SOR[7] - LED_2 SOR[8] - LED_0 SOR[9] - GPIO |

7.7.57 CHIP_SOR_2 Register (Address = 0x468) [reset = 0x0]

CHIP_SOR_2 is shown in [Table 7-70](#).

Return to the [Summary Table](#).

Table 7-70. CHIP_SOR_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|-------------|
| 15-4 | RESERVED | R | 0x0 | Reserved |
| 3-0 | sor_19_16 | R | 0x0 | Reserved |

7.7.58 LEDS_CFG_2 Register (Address = 0x469) [reset = 0x0]

LEDS_CFG_2 is shown in [Table 7-71](#).

Return to the [Summary Table](#).

Table 7-71. LEDS_CFG_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|--|
| 15-11 | RESERVED | R | 0x0 | Reserved |
| 10 | led_2_polarity | R/W | 0x0 | LED_2 polarity: 0 - Active low 1 - Active high |
| 9 | led_2_drv_val | R/W | 0x0 | If bit #8 is set, this is the value of LED_2 |
| 8 | led_2_drv_en | R/W | 0x0 | 0 - LED_2 is in normal operation mode 1 - Drive the value of LED_2 (driven value is bit 9) |
| 7 | RESERVED | R | 0x0 | Reserved |
| 6 | led_1_polarity | R/W | 0x0 | LED_1 polarity: 0 - Active low 1 - Active high |
| 5 | led_1_drv_val | R/W | 0x0 | If bit #4 is set, this is the value of LED_1 |
| 4 | led_1_drv_en | R/W | 0x0 | 0 - LED_1 is in normal operation mode 1 - Drive the value of LED_1 (driven value is bit #5) |
| 3 | RESERVED | R | 0x0 | Reserved |
| 2 | led_0_polarity | R/W | 0x0 | LED_0 polarity: 0 - Active low 1 - Active high |
| 1 | led_0_drv_val | R/W | 0x0 | If bit #1 is set, this is the value of LED_1 |
| 0 | led_0_drv_en | R/W | 0x0 | 0 - LED_0 is in normal operation mode 1 - Drive the value of LED_0 (driven value is bit #1) |

7.7.59 AN_STAT_1 Register (Address = 0x60C) [reset = 0x0]

 AN_STAT_1 is shown in [Table 7-72](#).

 Return to the [Summary Table](#).

Table 7-72. AN_STAT_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 15 | master_slave_resol_fail | R | 0x0 | 1b = Master Slave resolution failed 0b = Master Slave resolution successful |
| 14-12 | an_state | R | 0x0 | |
| 11 | RESERVED | R | 0x0 | |
| 10-8 | hd_state | R | 0x0 | |
| 7 | RESERVED | R | 0x0 | |
| 6-4 | rx_state | R | 0x0 | |
| 3-0 | an_tx_state | R | 0x0 | |

7.7.60 dsp_reg_72 Register (Address = 0x872) [reset = 0x0]

 dsp_reg_72 is shown in [Table 7-73](#).

 Return to the [Summary Table](#).

Table 7-73. dsp_reg_72 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--------------------------------------|
| 15-10 | RESERVED | R | 0x0 | |
| 9-0 | mse_sqi | R | 0x0 | SQI : Reciever Avg Mean Square Value |

7.7.61 SCAN_2 Register (Address = 0xE01) [reset = 0x0]

 SCAN_2 is shown in [Table 7-74](#).

 Return to the [Summary Table](#).

Table 7-74. SCAN_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 15-9 | RESERVED | R | 0x0 | |
| 8-4 | scan_state_saf | R | 0x0 | |
| 3 | cfg_en_efuse_burn | R | 0x0 | Enable the switch in the power supply path for EFUSE module Note : This bit written by programming 0x0303 in 0x0E00 |
| 2-0 | RESERVED | R | 0x0 | |

7.7.62 PAM_PMD_CTRL_1 Register (Address = 0x1000) [reset = 0x0]

 PAM_PMD_CTRL_1 is shown in [Table 7-75](#).

 Return to the [Summary Table](#).

Table 7-75. PAM_PMD_CTRL_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|--|
| 15 | PMA_Reset | R | 0x0 | 1b = PMA/PMD reset 0b = Normal operation Note : Read write bit, self clearing Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. Please remove 0x1 from [15:12] while using the address. |
| 14-12 | RESERVED | R | 0x0 | |
| 11 | cfg_low_power | R | 0x0 | 1b = Low-power mode 0b = Normal operation Note : Read write bit Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 10-1 | RESERVED | R | 0x0 | |
| 0 | PMA_loopback | R | 0x0 | 1 = Enable loopback mode 0 = Disable loopback mode Note : Read write bit Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. Please remove 0x1 from [15:12] while using the address. |

7.7.63 PMA_PMD_CTRL_2 Register (Address = 0x1007) [reset = 0x3D]

PMA_PMD_CTRL_2 is shown in [Table 7-76](#).

Return to the [Summary Table](#).

Table 7-76. PMA_PMD_CTRL_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|------|-------|--|
| 15-6 | RESERVED | R | 0x0 | |
| 5-0 | cfg_pma_type_selection | R | 0x3D | 111101b = BASE-T1 type selection for device Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. Please remove 0x1 from [15:12] while using the address. |

7.7.64 PMA_PMD_EXTENDED_ABILITY_2 Register (Address = 0x100B) [reset = 0x800]

PMA_PMD_EXTENDED_ABILITY_2 is shown in [Table 7-77](#).

Return to the [Summary Table](#).

Table 7-77. PMA_PMD_EXTENDED_ABILITY_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 15-12 | RESERVED | R | 0x0 | |

Table 7-77. PMA_PMD_EXTENDED_ABILITY_2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|---|
| 11 | base_t1_extended_abilities | R | 0x1 | 1b = PMA/PMD has BASE-T1 extended abilities listed in register 1.18 0b = PMA/PMD does not have BASE-T1 extended abilities Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 10-0 | RESERVED | R | 0x0 | |

7.7.65 PMA_PMD_EXTENDED_ABILITY Register (Address = 0x1012) [reset = 0x4]

 PMA_PMD_EXTENDED_ABILITY is shown in [Table 7-78](#).

 Return to the [Summary Table](#).

Table 7-78. PMA_PMD_EXTENDED_ABILITY Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|------|-------|--|
| 15-4 | RESERVED | R | 0x0 | |
| 3 | RESERVED | R | 0x0 | Reserved |
| 2 | mr_10_base_t1l_ability | R | 0x1 | 1b = PMA/PMD is able to perform 10BASE-T1L 0b = PMA/PMD is not able to perform 10BASE-T1L Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 1 | RESERVED | R | 0x0 | Reserved |
| 0 | RESERVED | R | 0x0 | Reserved |

7.7.66 PMA_PMD_CTRL Register (Address = 0x1834) [reset = 0x4002]

 PMA_PMD_CTRL is shown in [Table 7-79](#).

 Return to the [Summary Table](#).

Table 7-79. PMA_PMD_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|---|
| 15 | RESERVED | R | 0x0 | |
| 14 | cfg_master_slave_val | R/W | 0x1 | 1b = Configure PHY as MASTER 0b = Configure PHY as SLAVE Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 13-4 | RESERVED | R | 0x0 | |
| 3-0 | cfg_type_selection | R | 0x2 | 0000b = Reserved 0001b = Reserved 0010b = 10BASE-T1L 0011b = Reserved 01xxb = Reserved 1xxxb = Reserved Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |

7.7.67 PMA_CTRL Register (Address = 0x18F6) [reset = 0x0]

PMA_CTRL is shown in [Table 7-80](#).

Return to the [Summary Table](#).

Table 7-80. PMA_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|---|
| 15 | PMA_Reset | R | 0x0 | 1 = PMA reset 0 = Normal operation Note : Read write bit, self clearing Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 14 | cfg_transmit_disable | R | 0x0 | 1 = Transmit disable 0 = Normal operation Note : Read write bit Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 13 | RESERVED | R | 0x0 | |
| 12 | cfg_incr_tx_lvl | R/W | 0x0 | 1 = Enable 2.4 Vpp operating mode 0 = Enable 1.0 Vpp operating mode Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 11 | cfg_low_power | R | 0x0 | 1 = Low-power mode 0 = Normal operation Note : Read write bit Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 10 | cfg_eee_enable | R/W | 0x0 | 1 = Enable EEE mode 0 = Disable EEE mode Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 9-1 | RESERVED | R | 0x0 | |
| 0 | PMA_loopback | R | 0x0 | 1 = Enable loopback mode 0 = Disable loopback mode Note : Read write bit Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |

ADVANCE INFORMATION

7.7.68 PMA_STATUS Register (Address = 0x18F7) [reset = 0x3000]

PMA_STATUS is shown in [Table 7-81](#).

Return to the [Summary Table](#).

Table 7-81. PMA_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 15-14 | RESERVED | R | 0x0 | |
| 13 | loopback_ability | R | 0x1 | 1 = PHY has loopback ability 0 = PHY has no loopback ability Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |

Table 7-81. PMA_STATUS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|-------|-------|---|
| 12 | tx_lvl_incr_ability | R | 0x1 | 1 = PHY has 2.4 Vpp operating mode ability 0 = PHY does not have 2.4 Vpp operating mode ability Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 11 | low_power_ability | R | 0x0 | 1 = PMA has low-power ability 0 = PMA does not have low-power ability Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 10 | eee_ability | R | 0x0 | 1 = PHY has EEE ability 0 = PHY does not have EEE ability Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 9 | receive_fault_ability | R | 0x0 | 1 = PMA has the ability to detect a fault condition on the receive path 0 = PMA does not have the ability to detect a fault condition on the receive path Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 8-3 | RESERVED | R | 0x0 | |
| 2 | receive_polarity | R | 0x0 | 1 = Receive polarity is reversed 0 = Receive polarity is not reversed Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 1 | receive_fault | R/W0C | 0x0 | 1 = Fault condition detected 0 = Fault condition not detected Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 0 | receive_link_status | R/W0S | 0x0 | 1 = PMA receive link up 0 = PMA receive link down Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |

ADVANCE INFORMATION

7.7.69 TEST_MODE_CTRL Register (Address = 0x18F8) [reset = 0x0]TEST_MODE_CTRL is shown in [Table 7-82](#).Return to the [Summary Table](#).

Table 7-82. TEST_MODE_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|--|
| 15-13 | cfg_test_mode | R/W | 0x0 | 1xb = Reserved 011b = Test mode 3 010b = Test mode 2 001b = Test mode 1 000b = Normal (non-test) operation Prefixed 0x1 in [15:12] of address to differentiate. Please remove 0x1 from [15:12] while using the address. |
| 12-0 | RESERVED | R | 0x0 | |

7.7.70 PCS_CTRL Register (Address = 0x3000) [reset = 0x0]

PCS_CTRL is shown in [Table 7-83](#).

Return to the [Summary Table](#).

Table 7-83. PCS_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|--|
| 15 | PCS_Reset | R | 0x0 | 1 = PCS reset 0 = Normal operation Note - RW bit, self clear bit Prefixed 0x3 in [15:12] of address to differentiate. Please remove 0x3 from [15:12] while using the address. |
| 14 | mmd3_loopback | R | 0x0 | 1 = Enable loopback mode 0 = Disable loopback mode Note - RW bit Prefixed 0x3 in [15:12] of address to differentiate. Please remove 0x3 from [15:12] while using the address. |
| 13-0 | RESERVED | R | 0x0 | |

7.7.71 PCS_CTRL_2 Register (Address = 0x38E6) [reset = 0x0]

PCS_CTRL_2 is shown in [Table 7-84](#).

Return to the [Summary Table](#).

Table 7-84. PCS_CTRL_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|--|
| 15 | PCS_Reset | R | 0x0 | 1 = PCS reset 0 = Normal operation Note - RW bit, self clear bit Prefixed 0x3 in [15:12] of address to differentiate. Please remove 0x3 from [15:12] while using the address. |
| 14 | mmd3_loopback | R | 0x0 | 1 = Enable loopback mode 0 = Disable loopback mode Note - RW bit Prefixed 0x3 in [15:12] of address to differentiate. Please remove 0x3 from [15:12] while using the address. |

Table 7-84. PCS_CTRL_2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 13-0 | RESERVED | R | 0x0 | |

7.7.72 PCS_STATUS Register (Address = 0x38E7) [reset = 0x0]

PCS_STATUS is shown in [Table 7-85](#).

Return to the [Summary Table](#).

Table 7-85. PCS_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|-------|-------|---|
| 15-12 | RESERVED | R | 0x0 | |
| 11 | tx_lpi_received | R/W0C | 0x0 | 1 = Tx PCS has received LPI 0 = LPI not received Prefixed 0x3 in [15:12] of address to differentiate. Please remove 0x3 from [15:12] while using the address. |
| 10 | rx_lpi_received | R/W0C | 0x0 | 1 = Rx PCS has received LPI 0 = LPI not received Prefixed 0x3 in [15:12] of address to differentiate. Please remove 0x3 from [15:12] while using the address. |
| 9 | tx_lpi_indication | R | 0x0 | 1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI Prefixed 0x3 in [15:12] of address to differentiate. Please remove 0x3 from [15:12] while using the address. |
| 8 | rx_lpi_indication | R | 0x0 | 1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI Prefixed 0x3 in [15:12] of address to differentiate. Please remove 0x3 from [15:12] while using the address. |
| 7 | fault | R/W0C | 0x0 | 1 = Fault condition detected 0 = No fault condition detected Prefixed 0x3 in [15:12] of address to differentiate. Please remove 0x3 from [15:12] while using the address. |
| 6-3 | RESERVED | R | 0x0 | |
| 2 | receive_link_status | R/W0S | 0x0 | 1 = PCS receive link up 0 = PCS receive link down Prefixed 0x3 in [15:12] of address to differentiate. Please remove 0x3 from [15:12] while using the address. |
| 1-0 | RESERVED | R | 0x0 | |

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

When using the device for Ethernet applications, it is necessary to meet certain requirements for normal operation. The following subsections are intended to assist in appropriate component selection and required circuit connections.

8.2 Typical Applications

Figure 8-1 shows a typical application for the DP83TD510E.

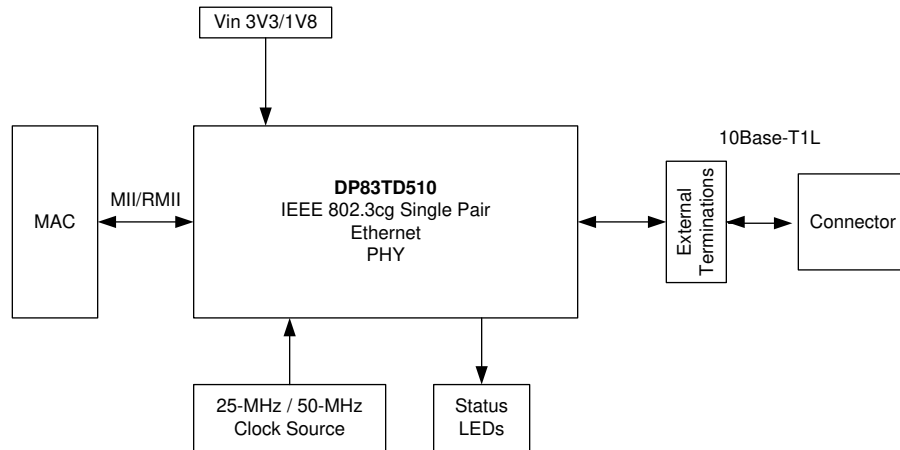


Figure 8-1. Typical DP83TD510E Application

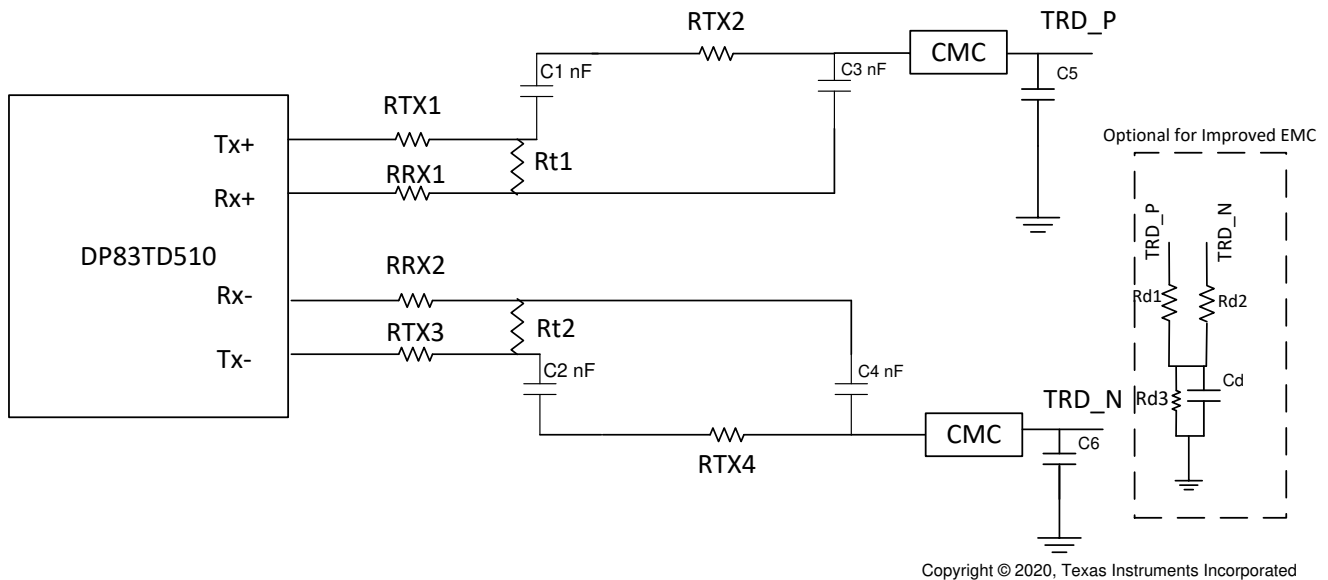
8.2.1 Termination Circuit

DP83TD510E is expected to be used in Intrinsic Safe and non Intrinsic Safe Applications. Please refer to appropriate termination circuit based on the application needs, see [Figure 8-2](#) .

Note

Termination circuit and passive values are initial estimates and subject to change

8.2.1.1 Termination Circuit for Intrinsic Safe Applications



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Figure 8-2. Termination Circuit for Intrinsic Safe Applications

Table 8-1. Termination Circuit Component Value for Intrinsic Safe Applications

| Applications | 1v p2p Intrinsic Safe Config 1 | 1v p2p Intrinsic Safe Config 2 |
|------------------|---------------------------------------|---------------------------------------|
| 1 RTX1, RTX3 | 26.5 | 50 |
| 2 RTX2, RTX4 (Ω) | 23.5 | 0 |
| 3 RRX1, RRX2 (Ω) | 2K | 2K |
| 4 Rt1(Ω) | NC | 0 |
| 5 Rt2(Ω) | NC | 0 |
| 6 Rd1(Ω) | 1K | 1K |
| 7 Rd2(Ω) | 1K | 1K |
| 8 Rd3(Ω) | 160K | 160K |
| 9 C1 | 230 nF | 230 nF |
| 10 C2 | 230 nF | 230 nF |
| 11 C3 | 5 nF | NC |
| 12 C4 | 5 nF | NC |
| 13 C5 | 100 pF < C < 400 pF (default: 100 pF | 100 pF < C < 400 pF (default: 100 pF |
| 14 C6 | 100 pF < C < 400 pF (default: 100 pF | 100 pF < C < 400 pF (default: 100 pF |
| 15 Cd | 0.01 uF | 0.01 uF |

Please ensure over all impedance on the Transmitter shall be 50Ω. If additional components on path adding the impedance, it shall be compensated by reducing Rtx1/Rtx3.

8.2.1.2 Components Range for Power Coupling/Decoupling

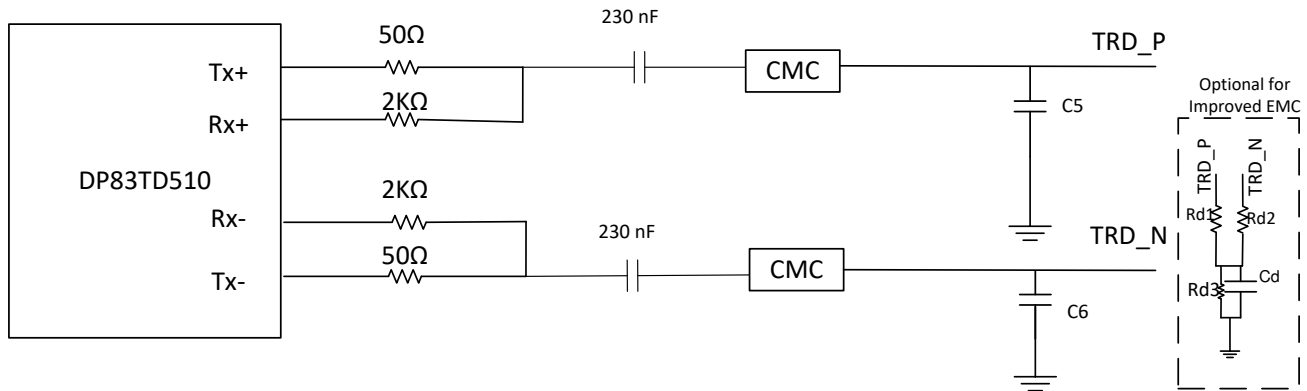
Below table provides recommended component ranges for Power/Data decoupling network

Table 8-2. Recommended Components Range for Power Coupling/Decoupling

| | Components | Range |
|---|--|--|
| 1 | Cap of ESD diode between MDI lines (Surge protection) | < 100 pF (Differential Cap) |
| 2 | Cap of TVS Diode (MDI line to ground)* | < 75 pF |
| 3 | Cap of Clamping Diodes (parallel to power coupling inductor) | < 50 pF |
| 4 | Power coupling inductor | <ul style="list-style-type: none"> Inductance 500 uH < L < 1.5 mH, DC Resistance < 200 mΩ |
| 5 | Cap of Rectifier Diodes | <50 pF |

8.2.1.3 Termination Circuit for Non-Intrinsic Safe Applications

Following termination circuit is recommended for application in non intrinsic safe application like in Building Automation, Factory Automation etc



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Figure 8-3. Termination Circuit for Non-Intrinsic Safe Applications

8.2.1.4 CMC Specifications

Table 8-3. CMC Specifications

| Parameters | Range |
|--------------------|----------|
| Inductance | 450 uH |
| Leakage Inductance | < 500 nH |
| DC Resistance | < 200 mΩ |

8.2.2 Design Requirements

The design requirements for the DP83TD510E are:

1. AVD Supply = 3.3 V
2. VDDIO Supply = 3.3 V or 1.8 V
3. Reference Clock Input = 25 MHz or 50 MHz (RMII Slave)

8.2.2.1 Clock Requirements

The DP83TD510E supports an external CMOS-level oscillator source or an internal oscillator with an external crystal.

8.2.2.1.1 Oscillator

If an external clock source is used, XI should be tied to the clock source and XO should be left floating. The amplitude of the oscillator should be a nominal voltage of VDDIO.

8.2.2.1.2 Crystal

The use of a 25-MHz, parallel resonant, 20-pF load crystal is recommended if operating with a crystal. A typical connection diagram is shown below for a crystal resonator circuit. The load capacitor values will vary with the crystal vendors; check with the vendor for the recommended loads.

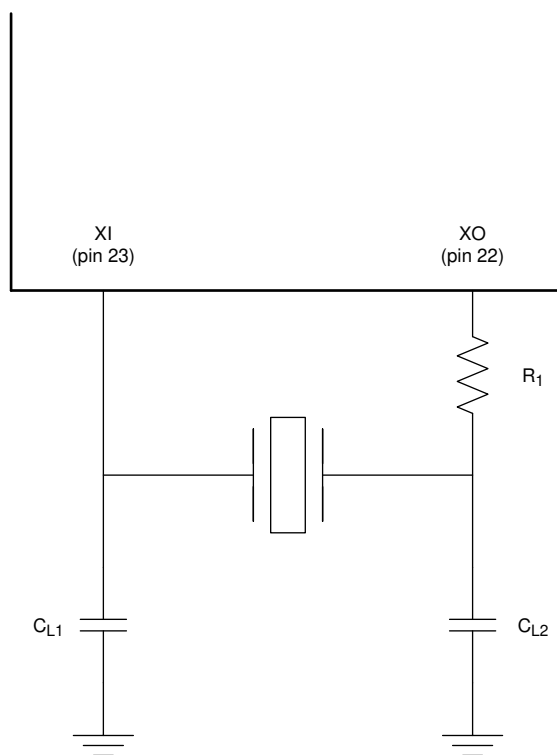


Figure 8-4. Crystal Oscillator Circuit

Table 8-4. 25-MHz Crystal Specification

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|------|-----|-----|------|
| Frequency | | | 25 | | MHz |
| Frequency Tolerance | Including all parameters (Temperature, aging etc) | -100 | | 100 | ppm |
| Load Capacitance | | | 15 | 30 | pF |
| ESR | | | 50 | 150 | Ohm |

9 Power Supply Recommendations

The DP83TD510E is capable of operating from Single Supply 3V3. It supports single supply operations from 1V8 for Short Reach (1v p2p) mode. It also supports Dual Supply Operations for Lowest Power Dissipation. It also supports VDDIO to work at 3.3-V, 2.5-V or 1.8-V supply voltages PHY has capability to detect the power supply levels automatically for both AVDD and VDDIO..

Single Power Supply Operations : Analog supply shall be powered by 3.3 V or 1.8 V. AVDD of 3V3 can support both Long Reach (2.4-v p2p) and Short Reach(1-v p2p).

Please note with AVDD 1.8 V, only Short Cable mode of 1-V p2p will be supported.

Appropriate straps shall be configured to ensure Auto Negotiation transmits the correct capabilities of the PHY.

The recommended power supply de-coupling network is shown below:

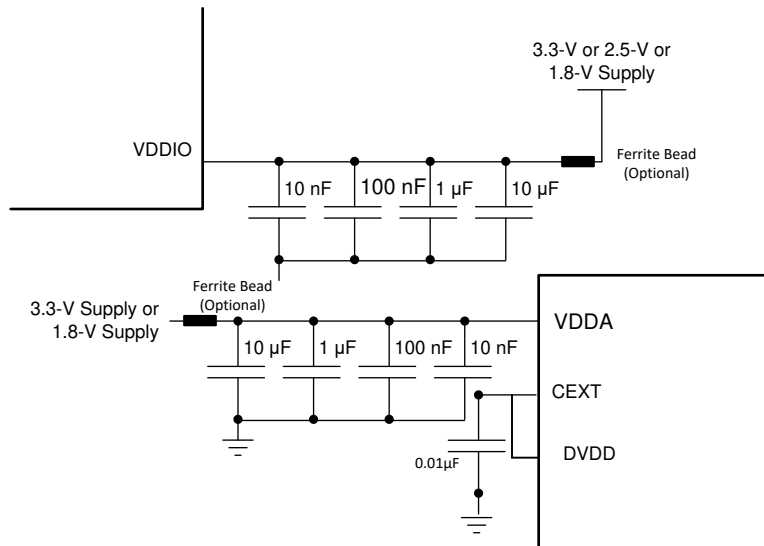


Figure 9-1. DP83TD510E Single Power Supply Decoupling Recommendation

For Dual Supply Operations, digital voltage rail of 1.0 V externally shall be supplied separately. This help reduce the power consumption further of the DP83TD510E. See below connections for Dual Power Supply.

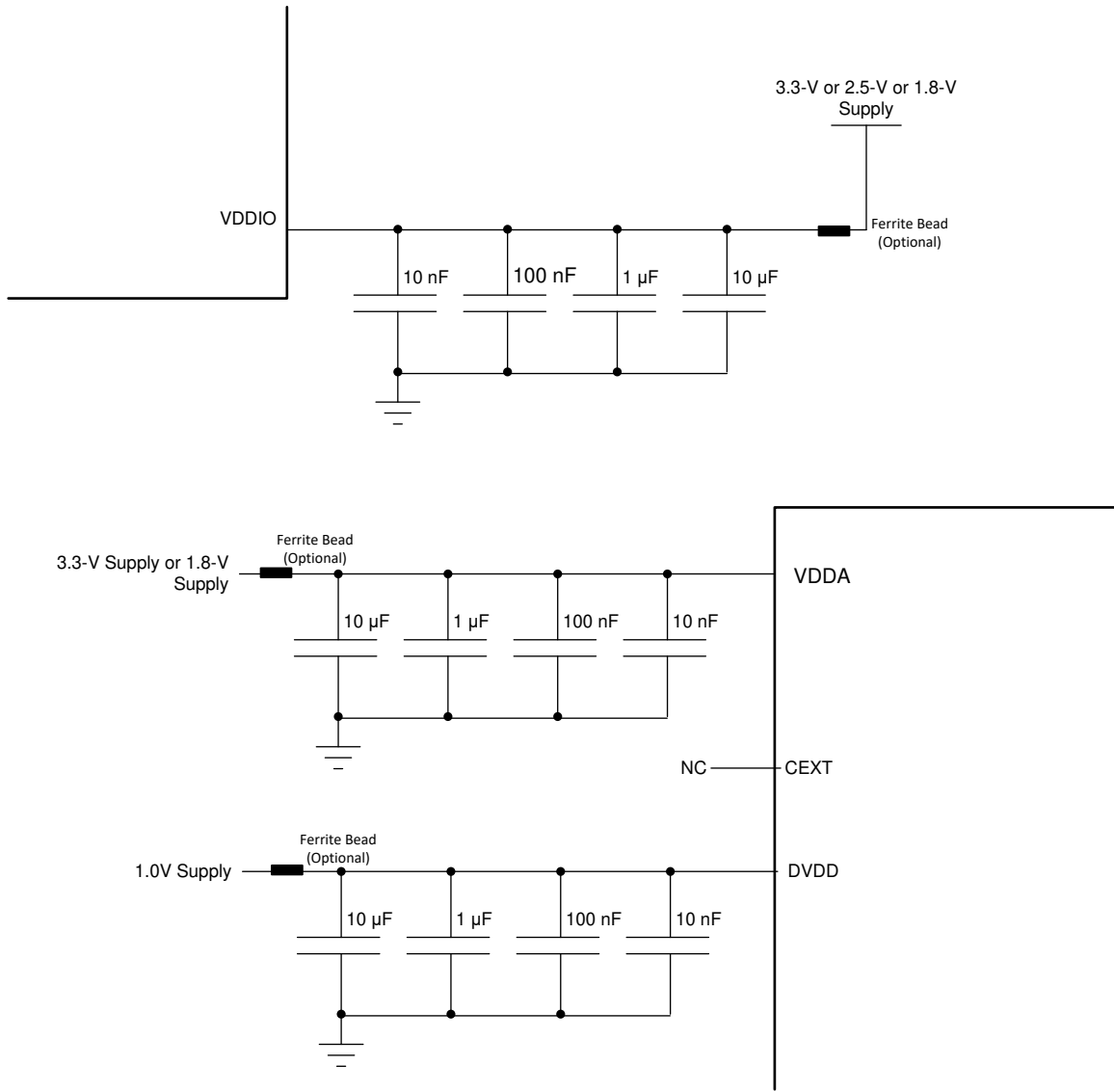


Figure 9-2. DP83TD510E Dual Supply Power Supply Decoupling Recommendation

10 Layout

10.1 Layout Guidelines

10.1.1 Signal Traces

PCB traces are lossy and long traces can degrade signal quality. Keep traces as short as possible. Unless mentioned otherwise, all signal traces must be 50- Ω single-ended impedance. Differential traces must 100- Ω differential. Take care to ensure impedance is controlled throughout. Impedance discontinuities cause reflections leading to emissions and signal integrity issues. Stubs should be avoided on all signal traces, especially differential signal pairs.

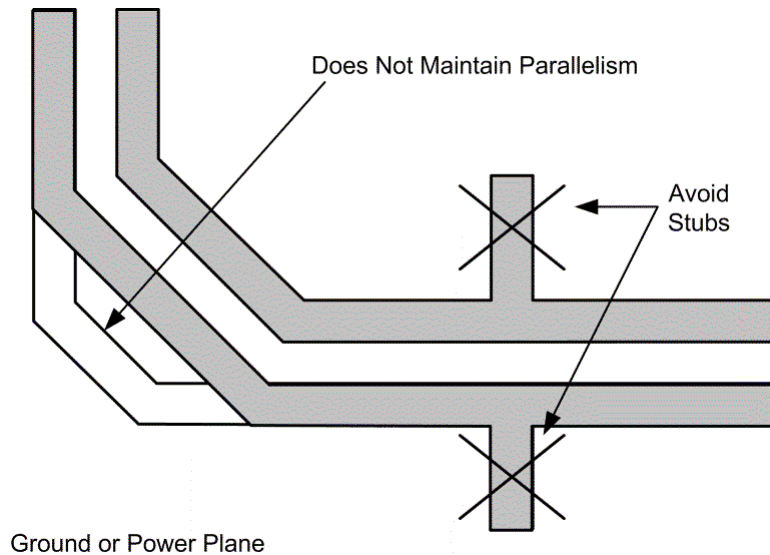


Figure 10-1. Differential Signal Traces

Within the differential pairs, trace lengths should be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and emissions. Length matching is also important for MAC interface connections. All RMII transmit signal traces should be length matched to each other and all RMII receive signal traces should be length matched to each other.

Ideally, there should be no crossover or vias on signal path traces. Vias present impedance discontinuities and should be minimized when possible. Route trace pairs on the same layer. Signals on different layers should not cross each other without at least one return path plane between them. Differential pairs should always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

10.1.2 Return Path

A general best practice is to have a solid return path beneath all MDI signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path between the signal traces should be avoided at all cost. A signal crossing a split plane may cause unpredictable return path currents and could impact signal quality and result in emissions issues.

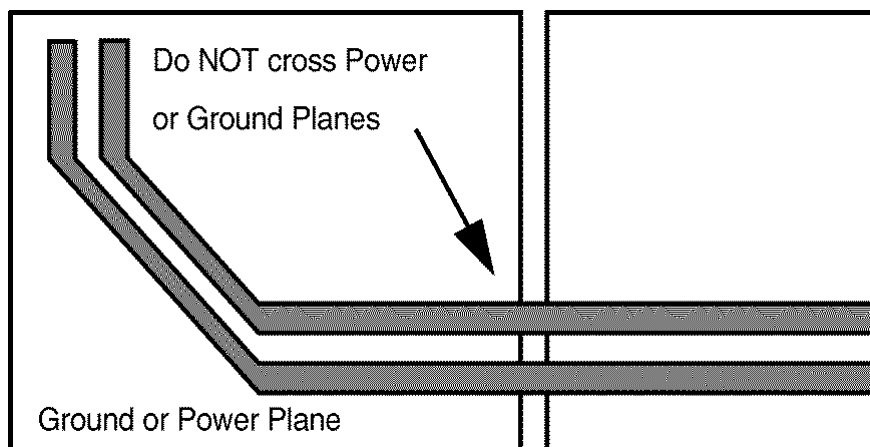


Figure 10-2. Differential Signal Pair and Plane Crossing

10.1.3 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

10.1.4 PCB Layer Stacking

To meet signal integrity and performance requirements, a minimum four-layer PCB is recommended. However, a six-layer PCB should be used when possible.

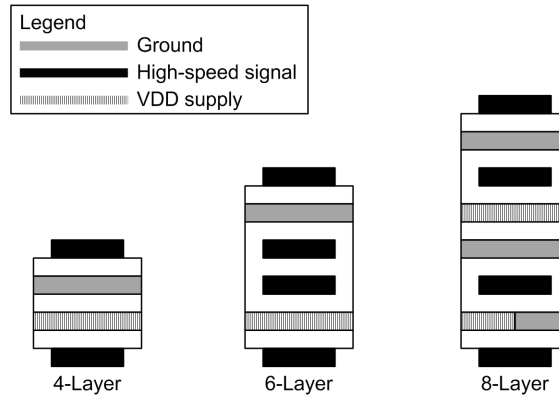


Figure 10-3. Recommended Layer Stack-Up

10.2 Layout Example

Please refer DP83TD510E EVM for information regarding layout.

11 Device and Documentation Support

11.1 Device Support

11.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

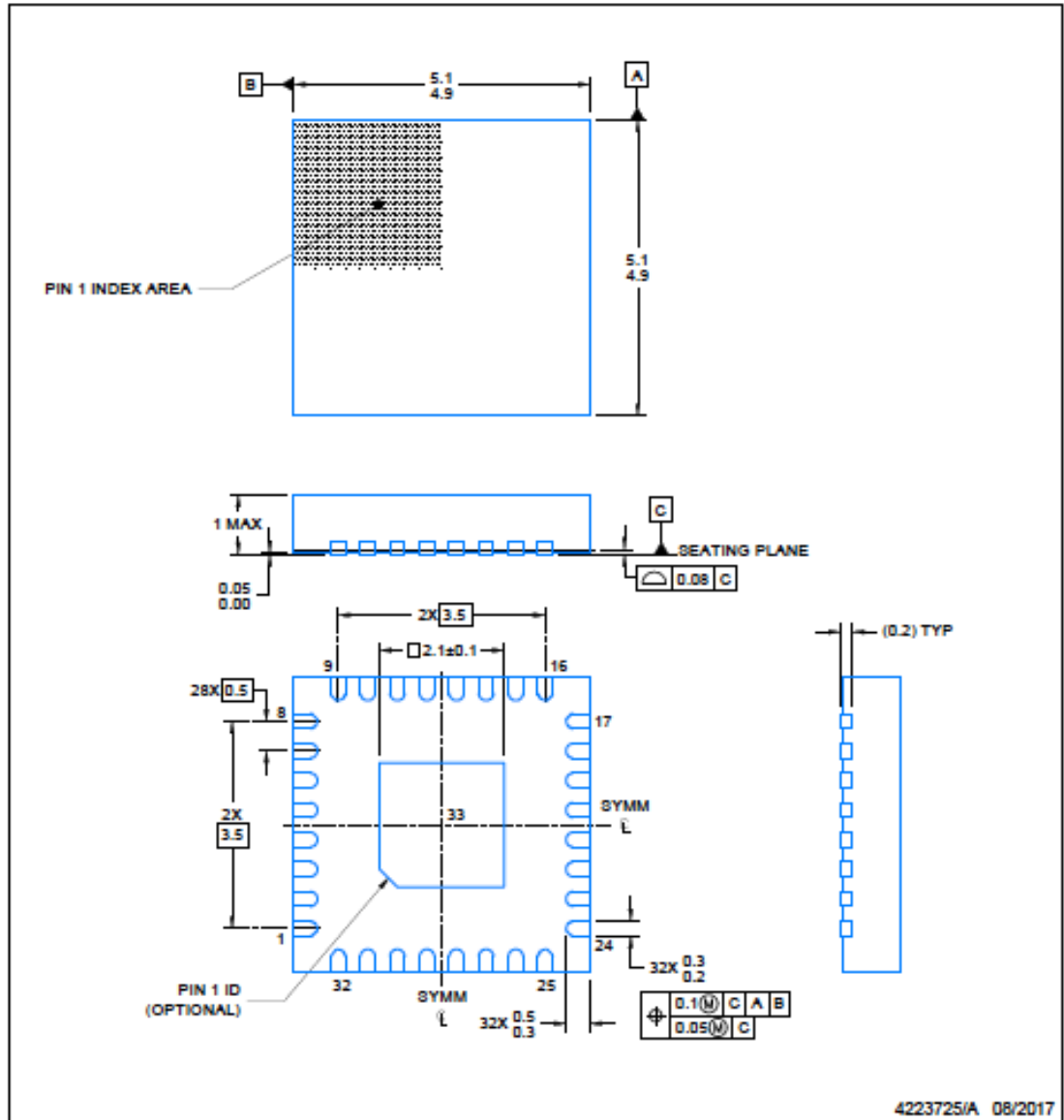
11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE **RHB0032M** **VQFN - 1 mm max height** PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

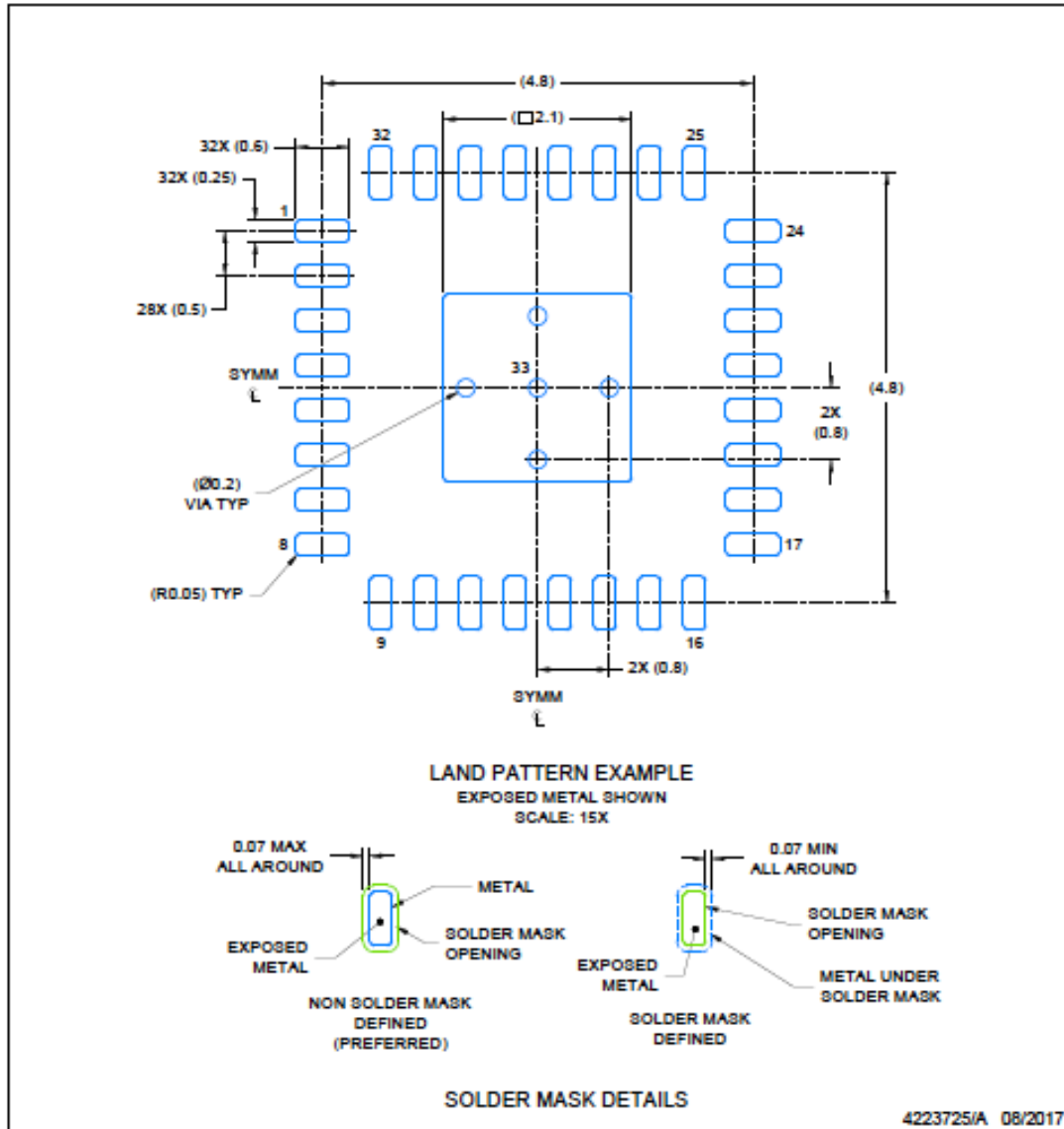
Figure 12-1. DP83TD510E Package Drawing

EXAMPLE BOARD LAYOUT

VQFN - 1 mm max height

RHB0032M

PLASTIC QUAD FLATPACK-NO LEAD

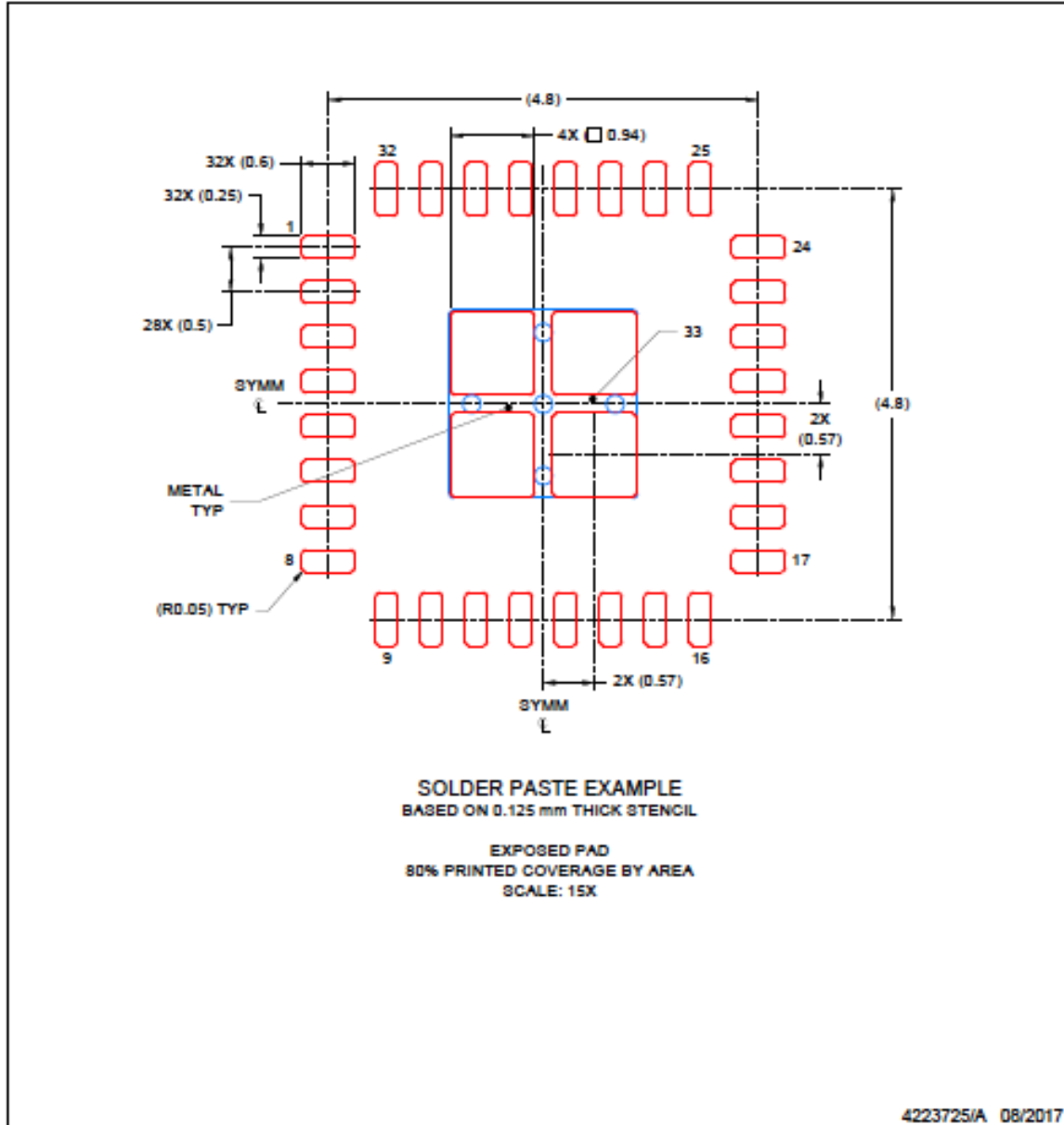


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

Figure 12-2. DP83TD510E Package Drawing

EXAMPLE STENCIL DESIGN
RHB0032M **VQFN - 1 mm max height**
PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Figure 12-3. DP83TD510E Package Drawing

ADVANCE INFORMATION

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| DP83TD510ERHBR | PREVIEW | VQFN | RHB | 32 | 3000 | TBD | Call TI | Call TI | -40 to 105 | | |
| DP83TD510ERHBT | PREVIEW | VQFN | RHB | 32 | 250 | TBD | Call TI | Call TI | -40 to 105 | | |
| PDP83TD510ERHBR | ACTIVE | VQFN | RHB | 32 | 3000 | TBD | Call TI | Call TI | -40 to 105 | | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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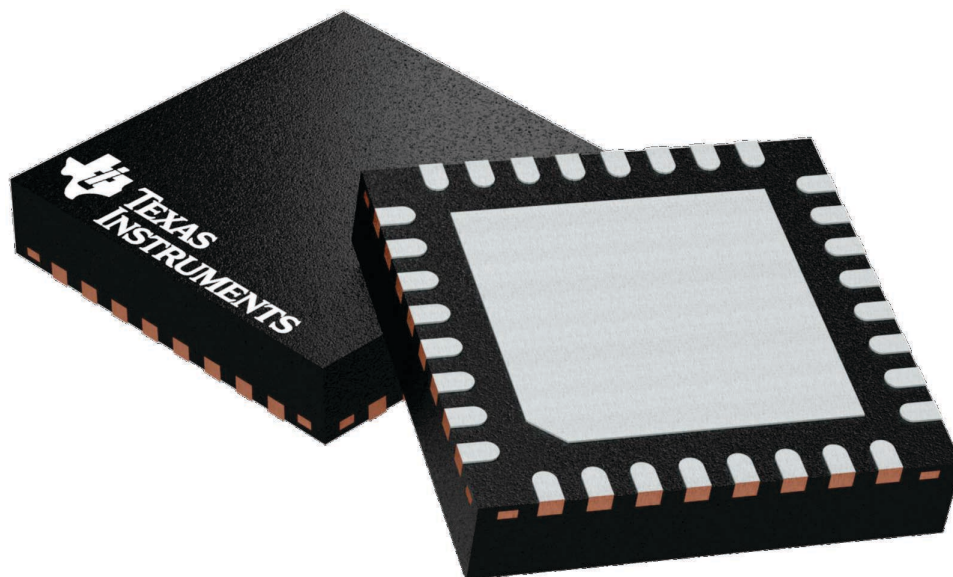
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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